64MBit Virtual Channel SDRAM

1 Advanced Information

- Fully Standard Synchronous Dynamic RAM, with all signals referenced to a positive clock edge
- Dual internal banks controlled by Bank Select Address
- Sixteen Channels controlled by Channel Select Address
- One Channel for write buffer (Dummy Channel)
- Quad segments controlled by Segment Select Address
- Byte control (x16) by LDQM and UDQM
- Programmable Wrap sequence (Sequential / Interleave)
- Programmable burst length (1, 2, 4, 8 and 16)
- Read latency (1, 2)
- Prefetch Read latency (4)
- Auto precharge and without auto precharge
- Auto refresh and Self refresh
- x4, x8, x16 organization
- Single 3.3 V ± 0.3 V power supply
- Interface: LVTTL
- Refresh cycle: 4 K cycles / 64 ms

1.1 Description

The 64M-bit Virtual Channel (VC) SDRAM is implemented to be 100% pin and package compatible to the industry standard SDRAM. It uses the same command protocol and interface as SDRAM. The VC SDRAM command set is a superset of the SDRAM. It also follows the same electrical and timing specifications of the SDRAM, such that it is possible for one product platform to be used with the VC SDRAM and non-VC SDRAM part.

1.2 Ordering Information

Table 1
Order Code VC SDRAM

Device Type	Partnumber	Q-Number	Packing	Note
16M x 4 SDRAM VCM LVTTL 143Mhz	HYB39V64400T -7		Trays	1
8M x 8 SDRAM VCM LVTTL 143Mhz	HYB39V64800T -7		Trays	1
4M x 16 SDRAM VCM LVTTL 143Mhz	HYB39V64160T -7		Trays	1
16M x 4 SDRAM VCM SSTL 143Mhz	HYB39V644402T -7		Trays	1
8M x 8 SDRAM VCM SSTL 143Mhz	HYB39V64802T -7		Trays	1
4M x 16 SDRAM VCM SSTL 143Mhz	HYB39V64162T -7		Trays	1
16M x 4 SDRAM VCM LVTTL 133Mhz	HYB39V644400T -7.5		Trays	
8M x 8 SDRAM VCM LVTTL 133Mhz	HYB39V64800T -7.5		Trays	
4M x 16 SDRAM VCM LVTTL 133Mhz	HYB39V64160T -7.5		Trays	
16M x 4 SDRAM VCM SSTL 133Mhz	HYB39V644402T -7.5		Trays	
8M x 8 SDRAM VCM SSTL 133Mhz	HYB39V64802T -7.5		Trays	
4M x 16 SDRAM VCM SSTL 133Mhz	HYB39V64162T -7.5		Trays	
16M x 4 SDRAM VCM LVTTL 100Mhz	HYB39V644400T -10		Trays	
8M x 8 SDRAM VCM LVTTL 100Mhz	HYB39V64800T -10		Trays	
4M x 16 SDRAM VCM LVTTL 100Mhz	HYB39V64160T -10		Trays	
16M x 4 SDRAM VCM SSTL 100Mhz	HYB39V644402T -10		Trays	
8M x 8 SDRAM VCM SSTL 100Mhz	HYB39V64802T -10		Trays	
4M x 16 SDRAM VCM SSTL 100Mhz	HYB39V64162T -10		Trays	
16M x 4 SDRAM VCM LVTTL 66Mhz	HYB39V644400T -15		Trays	
8M x 8 SDRAM VCM LVTTL 66Mhz	HYB39V64800T -15		Trays	
4M x 16 SDRAM VCM LVTTL 66Mhz	HYB39V64160T -15		Trays	
16M x 4 SDRAM VCM SSTL 66Mhz	HYB39V644402T -15		Trays	
8M x 8 SDRAM VCM SSTL 66Mhz	HYB39V64802T -15		Trays	
4M x 16 SDRAM VCM SSTL 66Mhz	HYB39V64162T -15		Trays	

Note: 1: Under development

Table 2
Order Code Low Power VC SDRAM

Device Type	Partnumber	Q-Number	Packing	Note
16M x 4 SDRAM VCM LVTTL 143Mhz	HYB39V64400TL -7		Trays	1
8M x 8 SDRAM VCM LVTTL 143Mhz	HYB39V64800TL -7		Trays	1
4M x 16 SDRAM VCM LVTTL 143Mhz	HYB39V64160TL -7		Trays	1
16M x 4 SDRAM VCM SSTL 143Mhz	HYB39V644402TL -7		Trays	1
8M x 8 SDRAM VCM SSTL 143Mhz	HYB39V64802TL -7		Trays	1
4M x 16 SDRAM VCM SSTL 143Mhz	HYB39V64162TL -7		Trays	1
16M x 4 SDRAM VCM LVTTL 133Mhz	HYB39V644400TL -7.5		Trays	1
8M x 8 SDRAM VCM LVTTL 133Mhz	HYB39V64800TL -7.5		Trays	1
4M x 16 SDRAM VCM LVTTL 133Mhz	HYB39V64160TL -7.5		Trays	1
16M x 4 SDRAM VCM SSTL 133Mhz	HYB39V644402TL -7.5		Trays	1
8M x 8 SDRAM VCM SSTL 133Mhz	HYB39V64802TL -7.5		Trays	1
4M x 16 SDRAM VCM SSTL 133Mhz	HYB39V64162TL -7.5		Trays	1
16M x 4 SDRAM VCM LVTTL 100Mhz	HYB39V644400TL -10		Trays	1
8M x 8 SDRAM VCM LVTTL 100Mhz	HYB39V64800TL -10		Trays	1
4M x 16 SDRAM VCM LVTTL 100Mhz	HYB39V64160TL -10		Trays	1
16M x 4 SDRAM VCM SSTL 100Mhz	HYB39V644402TL -10		Trays	1
8M x 8 SDRAM VCM SSTL 100Mhz	HYB39V64802TL -10		Trays	1
4M x 16 SDRAM VCM SSTL 100Mhz	HYB39V64162TL -10		Trays	1
16M x 4 SDRAM VCM LVTTL 66Mhz	HYB39V644400TL -15		Trays	1
8M x 8 SDRAM VCM LVTTL 66Mhz	HYB39V64800TL -15		Trays	1
4M x 16 SDRAM VCM LVTTL 66Mhz	HYB39V64160TL -15		Trays	1
16M x 4 SDRAM VCM SSTL 66Mhz	HYB39V644402TL -15		Trays	1
8M x 8 SDRAM VCM SSTL 66Mhz	HYB39V64802TL -15		Trays	1
4M x 16 SDRAM VCM SSTL 66Mhz	HYB39V64162TL -15		Trays	1

Note: 1. All Low Power Products are under development

Table 3
Technical Code VC SDRAM

Partnumber	Organisation	Clock Frequency	Read Latency	Prefetch Read Latency	Channels	Interface	Package
HYB39V64400T -7	8M x 4 x 2	143 Mhz	2	4	16	LV TTL	Plastic TSOP
HYB39V64800T -7	Q67100-Q2663-N	143 Mhz	2	4	16	LV TTL	Plastic TSOP
HYB39V64160T -7	Q67100-Q2664-N	143 Mhz	2	4	16	LV TTL	Plastic TSOP
HYB39V644402T -7	Q67100-Q	143 Mhz	2	4	16	SSTL	Plastic TSOP
HYB39V64802T -7	Q67100-Q	143 Mhz	2	4	16	SSTL	Plastic TSOP
HYB39V64162T -7	Q67100-Q	143 Mhz	2	4	16	SSTL	Plastic TSOP
HYB39V644400T -7.5	Q67100-Q2665-N	133 Mhz	2	4	16	LV TTL	Plastic TSOP
HYB39V64800T -7.5	Q67100-Q2666-N	133 Mhz	2	4	16	LV TTL	Plastic TSOP
HYB39V64160T -7.5	Q67100-Q2667-N	133 Mhz	2	4	16	LV TTL	Plastic TSOP
HYB39V644402T -7.5	Q67100-Q	133 Mhz	2	4	16	SSTL	Plastic TSOP
HYB39V64802T -7.5	Q67100-Q	133 Mhz	2	4	16	SSTL	Plastic TSOP
HYB39V64162T -7.5	Q67100-Q	133 Mhz	2	4	16	SSTL	Plastic TSOP
HYB39V644400T -10	Q67100-Q2668-N	100 Mhz	2	4	16	LV TTL	Plastic TSOP
HYB39V64800T -10	Q67100-Q2669-N	100 Mhz	2	4	16	LV TTL	Plastic TSOP
HYB39V64160T -10	Q67100-Q2670-N	100 Mhz	2	4	16	LV TTL	Plastic TSOP
HYB39V644402T -10	Q67100-Q	100 Mhz	2	4	16	SSTL	Plastic TSOP
HYB39V64802T -10	Q67100-Q	100 Mhz	2	4	16	SSTL	Plastic TSOP
HYB39V64162T -10	Q67100-Q	100 Mhz	2	4	16	SSTL	Plastic TSOP
HYB39V644400T -15	Q67100-Q2665-N	66 Mhz	1	4	16	LV TTL	Plastic TSOP
HYB39V64800T -15	Q67100-Q2666-N	66 Mhz	1	4	16	LV TTL	Plastic TSOP
HYB39V64160T -15	Q67100-Q2667-N	66 Mhz	1	4	16	LV TTL	Plastic TSOP
HYB39V644402T -15	Q67100-Q	66 Mhz	1	4	16	SSTL	Plastic TSOP
HYB39V64802T -15	Q67100-Q	66 Mhz	1	4	16	SSTL	Plastic TSOP
HYB39V64162T -15	Q67100-Q	66 Mhz	1	4	16	SSTL	Plastic TSOP

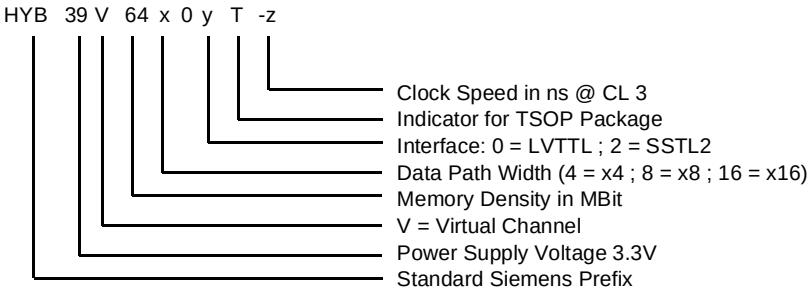
1.3 VC Nomenclature

Table 4
Product Partnumbers

Product Description	Siemens Partnumber	Interface
16M x 4	HYB 39 V 4400T -7/ -7.5/ -10/ -15	LV TTL
8M x 8	HYB 39 V 4400T -7/ -7.5/ -10/ -15	LV TTL
4M x 16	HYB 39 V 4400T -7/ -7.5/ -10/ -15	LV TTL
16M x 4	HYB 39 V 4400T -7/ -7.5/ -10/ -15	SSTL
8M x 8	HYB 39 V 4400T -7/ -7.5/ -10/ -15	SSTL
4M x 16	HYB 39 V 4400T -7/ -7.5/ -10/ -15	SSTL

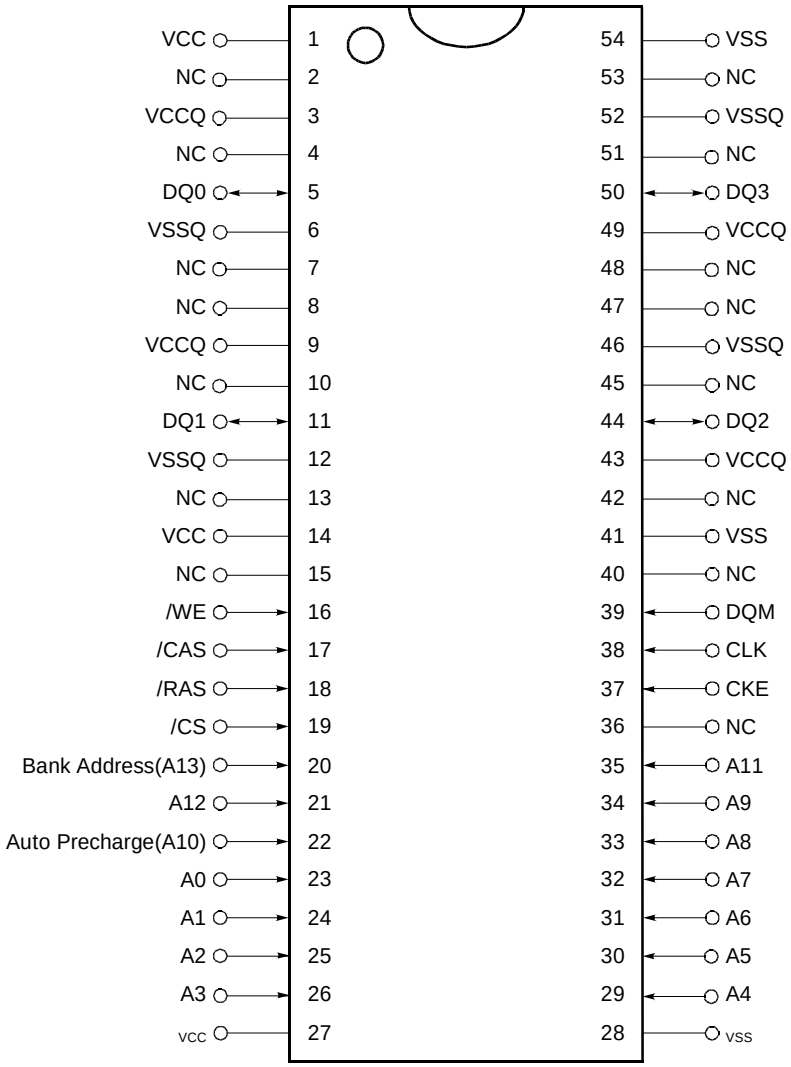
Table 5
Nomenclature of Product

Nomenclature



1.4 Pin Configurations

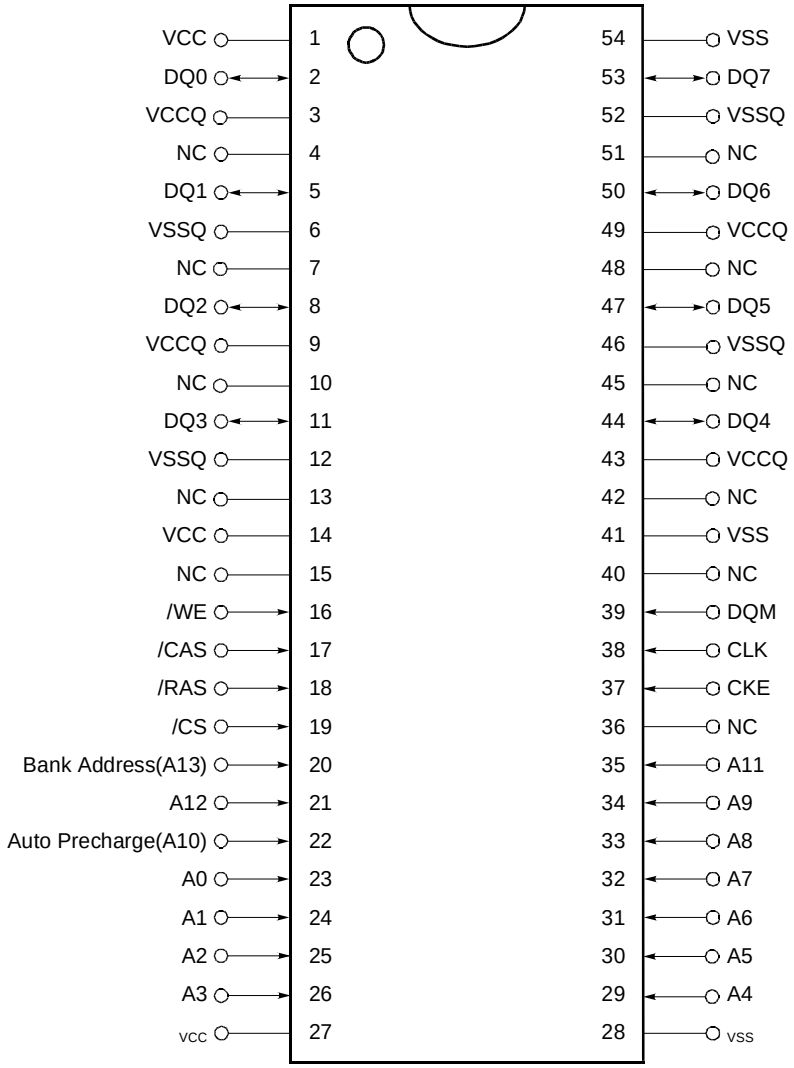
Figure 1
Pin Configuration HYB39V6440yT



A0 - A13	:	Address inputs	DQM	:	DQ mask enable
A0 - A12	:	Row address inputs	CKE	:	Clock enable
A0 - A7	:	Column address inputs	CLK	:	System clock input
DQ0 - DQ3	:	Data inputs/outputs	VCC	:	Supply voltage
/CS	:	Chip select	VSS	:	Ground
/RAS	:	Row address strobe	VCCQ	:	Supply voltage for DQ
/CAS	:	Column address strobe	VSSQ	:	Ground for DQ
/WE	:	Write enable	NC	:	No connection

Remark Refer to 1. Input/ Output Pin Function for Bank address, Channel address and Segment address

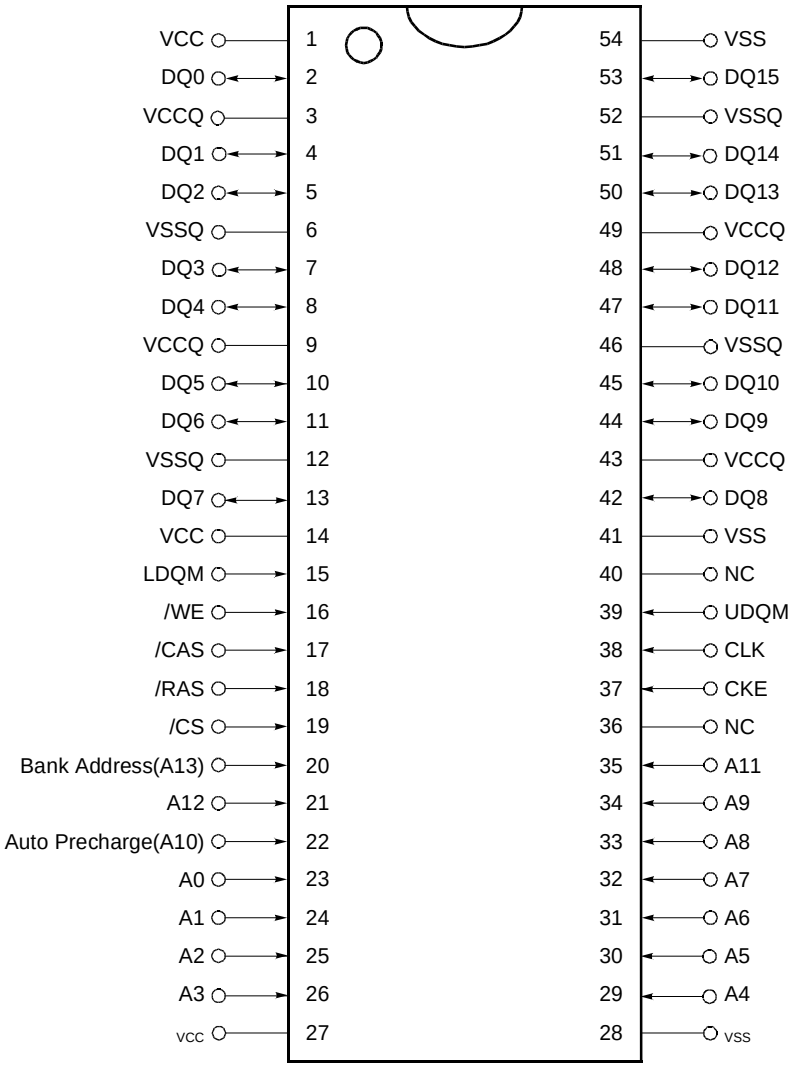
Figure 2
Pin Configuration HYB39V6480yT



A0 - A13	:	Address inputs	DQM	:	DQ mask enable
A0 - A12	:	Row address inputs	CKE	:	Clock enable
A0 - A6	:	Column address inputs	CLK	:	System clock input
DQ0 - DQ7	:	Data inputs/outputs	VCC	:	Supply voltage
/CS	:	Chip select	VSS	:	Ground
/RAS	:	Row address strobe	VCCQ	:	Supply voltage for DQ
/CAS	:	Column address strobe	VSSQ	:	Ground for DQ
/WE	:	Write enable	NC	:	No connection

Remark Refer to 1. Input/ Output Pin Function for Bank address, Channel address and Segment address

Figure 3
Pin Configuration HYB39V6416yT



A0 - A13	:	Address inputs	UDQM	:	Upper DQ mask enable
A0 - A12	:	Row address inputs	LDQM	:	Lower DQ mask enable
A0 - A5	:	Column address inputs	CKE	:	Clock enable
DQ0 - DQ15	:	Data inputs/outputs	CLK	:	System clock input
/CS	:	Chip select	VCC	:	Supply voltage
/RAS	:	Row address strobe	VSS	:	Ground
/CAS	:	Column address strobe	VCCQ	:	Supply voltage for DQ
/WE	:	Write enable	VSSQ	:	Ground for DQ
			NC	:	No connection

Remark Refer to 1. Input/ Output Pin Function for Bank address, Channel address and Segment address

2 Operation

2.1 VC SDRAM Architecture

The Virtual Channel Memory (VC Memory) is a memory core technology designed to improve memory data throughput efficiency and initial latency of memories. Intended for use in next generation memory systems, the VC Memory technology is ideal memory for a wide range of application such as Multimedia PC, Game machine, Internet Server etc…. The slow core operation memory such as DRAM, Flash Memory and Mask ROM can get very significant performance improvements with VC Memory technology.

Today's memory subsystems are accessed by multiple tasks/sources (memory masters), working in multitasking mode. Each memory master accesses memory with an address locality with a time locality, a block size and a number of contiguous accesses. Virtual Channel Memory architecture is designed for this multitasking, multiple masters, interleaving access scenarios. The VC Memory provides memory masters with Virtual Channels. Each channel is a set of resources that constitute a fast dedicated path for each memory masters to access the memory. The Virtual Channels will minimize the overhead resulting from other memory master's accesses, reduce the access latency and facilitate automatic data sharing.

Each channel is equipped with a data row buffer and its own independent operating modes. To the memory masters, this looks like its own very fast memory. The system memory controller associates these channels to the memory masters for their accesses. Thus, the channels are made to track the accesses of these memory masters. The system memory controller has complete controls over the operations of the channels. It can schedule and issue commands that causes segments of memory rows to be loaded into the channels or for data from the channels to be written back to the memory rows. Any channels can store the data from any rows, can be written to any rows and hence are fully associative. Then the Read and Write operations will be occurring as much as possible with these high speed channels, minimizing all overheads associated with the DRAM bank operations.

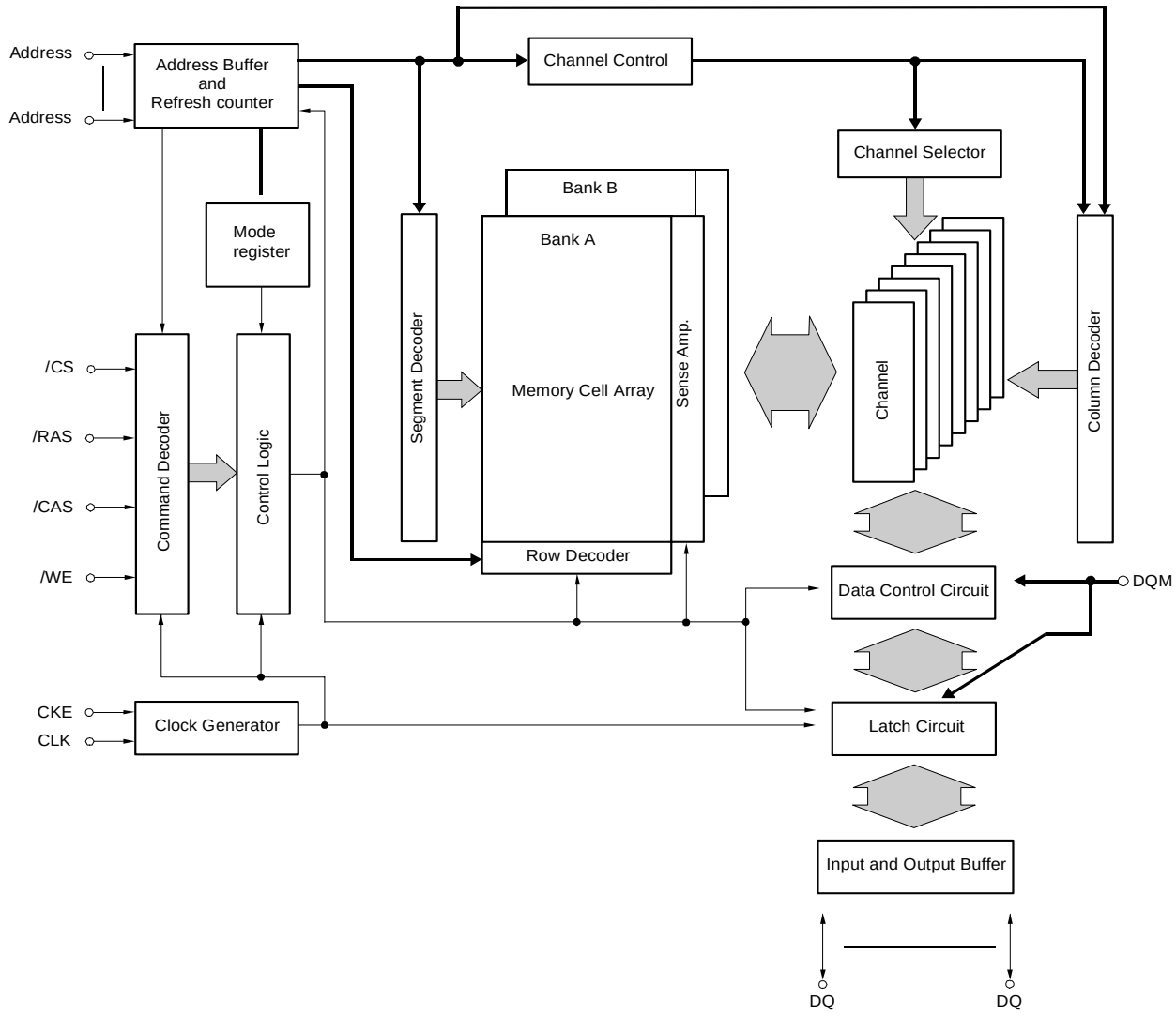
The Read/Write operations of the channels (foreground operations) can operate independently with the DRAM bank operations (background operations) of Activate, Precharge, Prefetch (Loading row data to channel) and Restore (Writing channel data to row). Then VC Memory also further enhances performance by allowing the system memory controller to schedule the foreground and background operations to operate concurrently.

VC DRAM architecture offers the following features and benefits:

- Multiplies the effective data throughput performance of conventional DRAM core.
- Achieving close to full data bus bandwidth with low latency, interleaved random row, random column Read/Write through the channels.
- Transparent DRAM bank operations through the concurrent foreground and Background Operations
- Very wide (128 bytes wide) internal data transfer bus between Channel and memory core
- Equivalence of tens of multiple memory banks by using only a fraction of the frequency of Row Activate and Precharge of conventional DRAM core.
- Fully associative, independent channel Row Buffer that can also be used as SRAM.

2.2 Block Diagramm

Figure 4
Block Diagramm Virtual Channel SDRAM



2.3 Concepts

Figure 5
Conceptual Schematics 1

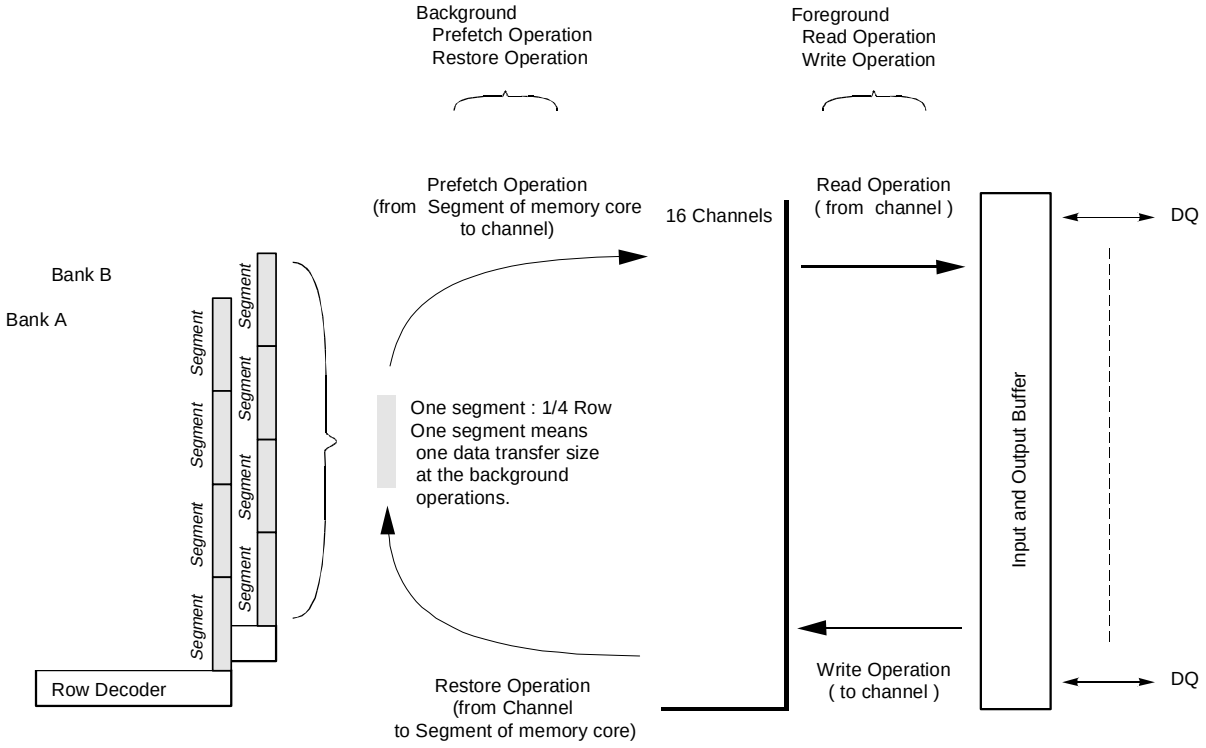
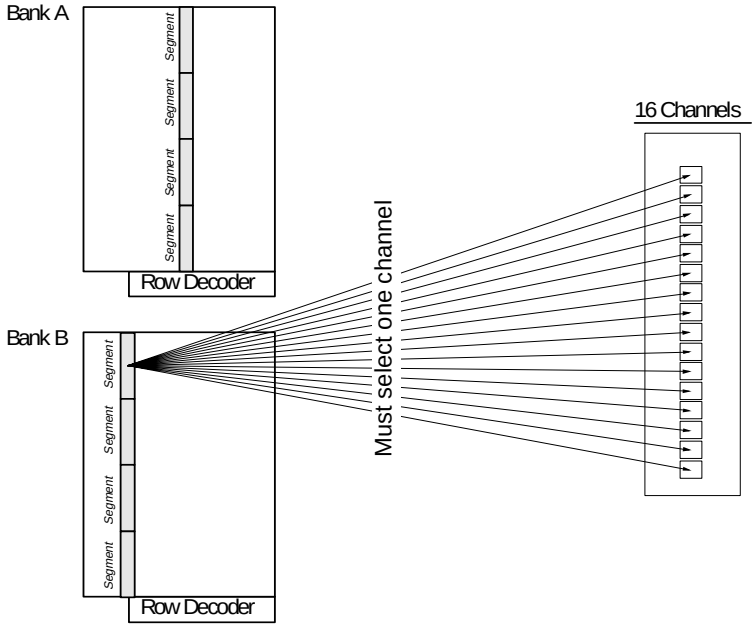


Figure 6
Conceptual Schematics 2

Prefetch Operation

The data is fetched from a segment to any channel buffer.



Restore Operation

The data is transferred from a channel buffer to any segment.

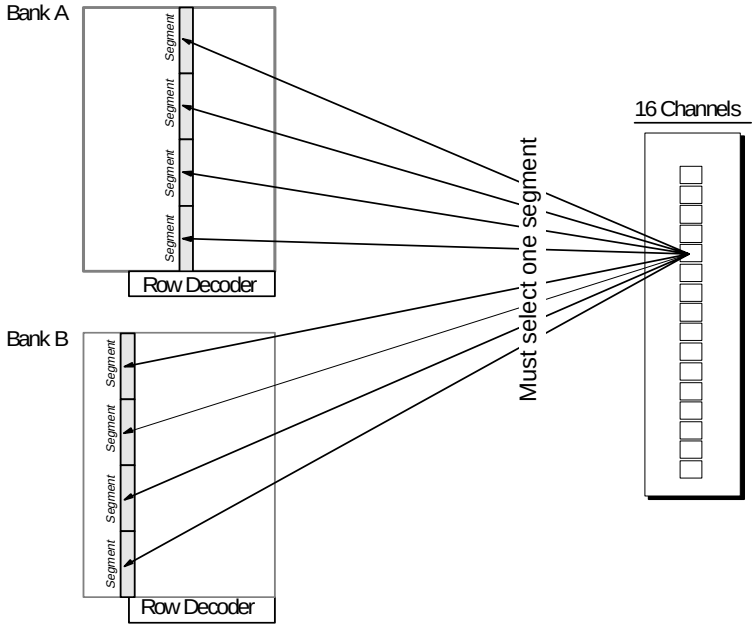
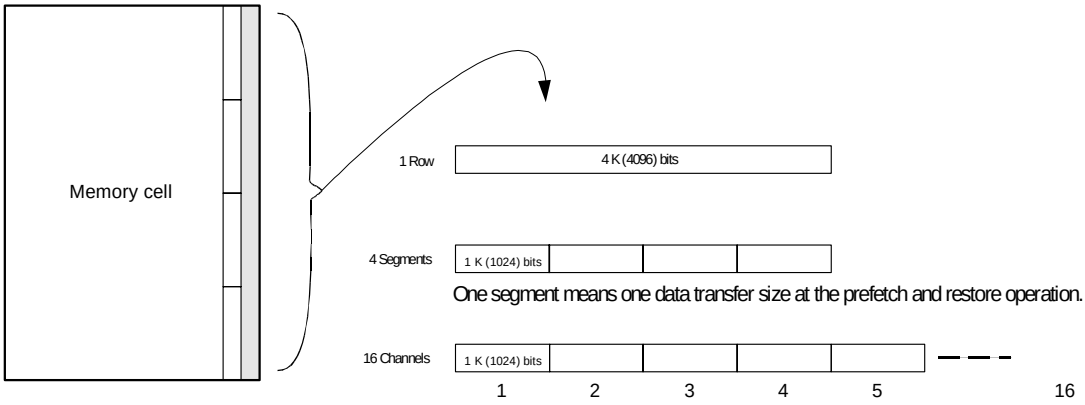
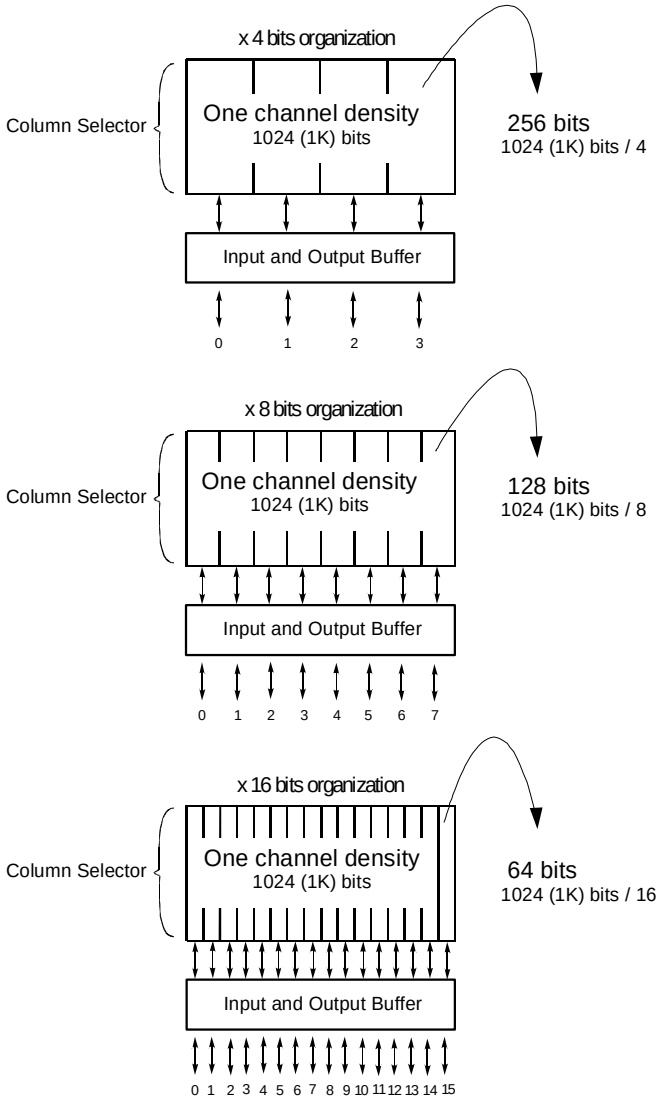


Figure 7
Data Size of Segment and Channel





2.4 IO Pins

Table 6
IO Pin Table 1

Pin name	Input/Output	Function
CLK	Input	CLK is the master clock input. Other inputs signals for all commands are referenced to the CLK rising edge.
CKE	Input	CKE determine validity of the next CLK (clock). If CKE is high, the next CLK rising edge is valid; otherwise it is invalid. If the CLK rising edge is invalid, the internal clock is not issued and the VC SDRAM suspends operation. When the VC SDRAM is not in burst mode and CKE is negated, the device enters power down mode. During power down mode, CKE must remain low.
/CS	Input	Chip select. /CS low starts the command input cycle, which occurs on rising edge of CLK. During /CS high, commands are ignored but operations continue.
/RAS, /CAS, /WE	Input	Command Inputs. The combination of these signals defines the command being entered. For details, refer to the Command Table in Command Functions. The symbol names (/RAS, /CAS, /WE) do not refer to the functional meanings used for conventional DRAM.
DQM For x8,x4 devices UDQM LDQM For x16 device	Input	For x4, x8 devices DQM controls I/O buffers. For x16 device UDQM and LDQM control upper byte and lower byte I/O buffers, respectively. **In read mode** DQM controls the output buffers like a conventional /OE pin. DQM high and DQM low turn the output buffers off and on, respectively. The DQM latency for the read is two clocks. **In write mode** DQM controls the word mask. Input data is written to the memory cell if DQM is low but not if DQM is high. The DQM latency for the write is zero.
DQ0 - DQ3 DQ0 - DQ7 DQ0 - DQ15	Input? /? Output	DQ pins have the same function as I/O pins on a Standard Synchronous DRAM. DQ0 - DQ3 (for x 4 device) DQ0 - DQ7 (for x 8 device) DQ0 - DQ15 (for x 16 device)
NC	–	No connect. Leave these pins unconnected.
VCC VSS	(Power supply)	VCC and VSS are power supply pins for internal circuits.
VCCQ VSSQ	(Power supply)	VCCQ and VSSQ are power supply pins for the output buffers.

Table 7
IO Pins Table 2

Pin name	Input? /? Output	Function
A0 - A13	Input	Address specification. These pins provide memory source and target addresses (bank, row, column, etc.), and channel addresses. **Row Address** Row Address is determined by A0 - A12 at the CLK (clock) rising edge in the active command cycle. It does not depend on the bit organization. **Column Address** Column Address is determined by A0 - A7 at the CLK rising edge in the read or write command cycle. It depends on the bit organization. : A0 - A7 for x4 device : A0 - A6 for x8 device : A0 - A5 for x16 device. **Bank Address(A13)** A13 is the bank select signal. In command cycle, A13 low select bank A, and A13 high select bank B. **Channel Address(A8, A9, A11, A12, A13)** A8, A9, A11, A12, A13 are the channel select signals. In prefetch, restore, read and write operations, channel is determined by A8, A9, A11, A12. In set register operation, channel is determined by A9, A10, A11, A12 and A13. **Segment Address(A0, A1, A10, A13)** A0, A1, A10, A13 are the segment select signals. In prefetch and restore operations, column address in channel is determined by A0, A1. In prefetch read operation, segment is determined by A10, A13. **Auto precharge Address(A10)** A10 defines the precharge mode. In the precharge command cycle High level: All banks are precharged. Low level: Only the bank selected by A13 is precharged. In the prefetch or restore command cycle High level: Auto precharge Low level: Without auto precharge

2.5 Truth Tables

2.5.1 Command Execution

All commands are executed with the signal combination at the rising edge of the clock (CLK), /CS (Chip Select) must be low at the command input cycle. CKE (Clock Enable) must be high at one clock before the command input cycle as shown in below. The state of the /RAS, /CAS, and /WE signals specifies the command function to be executed. Some commands have the same signal combination for /RAS, /CAS, and /WE and are distinguished by some of address Input signals. When /CS becomes high, operations continue as specified in the command, but further commands (signal states that would specify a command) are not registered until /CS becomes low. This state is Device deselect.

Figure 8
Device Deselect State

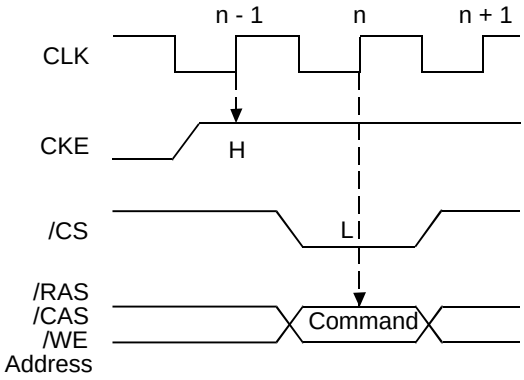


Table 8
Command Truth Table

Function	*Symbol*	*/CS*	*/RAS*	*/CAS*	*/WE*	*A13*	*A12*	*A11*	*A10*	*A9*	*A8*	*A7*	*A6*	*A5*	*A4*	*A3*	*A2*	*A1*	*A0*
Device deselect	DESL	H	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
No operation	NOP	L	H	H	H	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Prefetch without auto precharge	PFC	L	H	H	L	BA	Cha.	Cha.	L	Cha.	Cha.	L	L	L	x	x	x	Seg.	Seg.
Pair prefetch	PPF	L	H	H	L	BA	Cha.	Cha.	L	Cha.	Cha.	L	H	x	x	x	x	Seg.	Seg.
Prefetch to dummy without auto precharge	PFD	L	H	H	L	BA	x	x	x	x	x	L	L	H	x	x	x	Seg.	Seg.
Prefetch with auto precharge	PFCA	L	H	H	L	BA	Cha.	Cha.	H	Cha.	Cha.	L	L	L	x	x	x	Seg.	Seg.
Pair prefetch with auto precharge	PPFA	L	H	H	L	BA	Cha.	Cha.	H	Cha.	Cha.	L	H	x	x	x	x	Seg.	Seg.
Restore without auto precharge	RST	L	H	H	L	BA	Cha.	Cha.	L	Cha.	Cha.	H	x	x	x	x	x	Seg.	Seg.
Restore with auto precharge	RSTA	L	H	H	L	BA	Cha.	Cha.	H	Cha.	Cha.	H	x	x	x	x	x	Seg.	Seg.
Channel read	READ	L	H	L	H	x	Cha.	Cha.	x	Cha.	Cha.	Col.	Col.	Col.	Col.	Col.	Col.	Col.	Col.
Channel write	WRIT	L	H	L	L	L	Cha.	Cha.	x	Cha.	Cha.	Col.	Col.	Col.	Col.	Col.	Col.	Col.	Col.
Dummy channel write without auto restore	WRD	L	H	L	L	H	x	x	x	x	L	Col.	Col.	Col.	Col.	Col.	Col.	Col.	Col.
Dummy channel write with auto restore	WRDA	L	H	L	L	H	x	x	x	x	H	Col.	Col.	Col.	Col.	Col.	Col.	Col.	Col.
Bank activate	ACT	L	L	H	H	BA	Row	Row	Row	Row	Row	Row	Row	Row	Row	Row	Row	Row	Row
Prefetch read with auto precharge	PFR	L	L	H	L	Seg.	Cha.	Cha.	Seg.	Cha.	Cha.	Col.	Col.	Col.	Col.	Col.	Col.	Col.	Col.
Precharge selected bank	PRE	L	L	L	L	BA	x	x	L	x	x	x	x	L	x	x	x	x	x
Precharge all banks	PALL	L	L	L	L	x	x	x	H	x	x	x	x	L	x	x	x	x	x
Set register operation	SCLR	L	L	L	L	L	L	L	L	L	L	L	L	H	PRL	RL	RL	RL	WT
	SCCR	L	L	L	L	Cha.	Cha.	Cha.	Cha.	Cha.	L	L	H	H	x	x	BL	BL	BL

Abbreviations in the table mean as follows:

H : High level	L : Low level	X : High or Low level (Don't care)
Row : Row address	Col. : Column address	BA : Bank Address
Cha. : Channel address	Seg. : Segment address	
BL : Burst length	RL : Read Latency	PRL: Prefetch Read Latency

Table 9
CKE Truth Table

Current state	Function	Symbol	CKE n–1	CKE n	/CS	/RAS	/CAS	/WE	Address
Activating	Clock suspend mode entry	–	H	L	x	x	x	x	x
Any	Clock suspend	–	L	L	x	x	x	x	x
Clock suspend	Clock suspend mode exit	–	L	H	x	x	x	x	x
Idle	Auto refresh command	REF	H	H	L	L	L	H	x
Idle	Self refresh entry	SELF	H	L	L	L	L	H	x
Self refresh	Self refresh exit	–	L	H	L	H	H	H	x
			L	H	H	x	x	x	x
Idle	Power down entry	–	H	L	x	x	x	x	x
Power down	Power down exit	–	L	H	x	x	x	x	x

Remark H: High level, L: Low level, x: High or Low level (Don't care)

2.6 Commands

Table 10
Deselct Command

Device deselect (DESL)

/CS	/RAS	/CAS	/WE	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
High	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Remark x: High or Low level (Don't care)

The device is deselected by this command

Figure 9
Deselect Timing

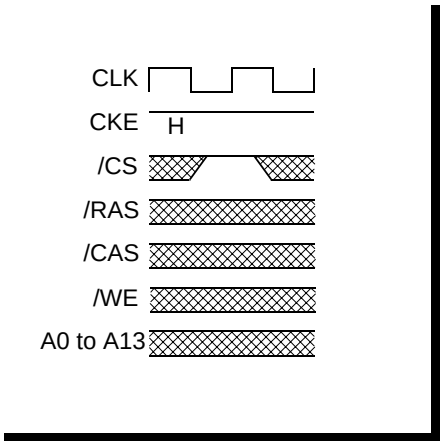


Table 11
NOP Command

/CS	/RAS	/CAS	/WE	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Low	High	High	High	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Remark x: High or Low level (Don't care)

This command is not a execution command. No operations begin or terminate by this command.

Figure 10
NOP Timing

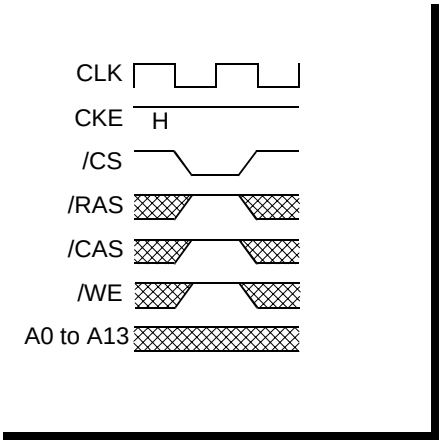


Table 12
Prefetch without Autoprecharge Command

Prefetch without auto precharge (PFC)

/CS	/RAS	/CAS	/WE	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Low	High	High	Low	BA	Cha.	Cha.	Low	Cha.	Cha.	Low	Low	Low	x	x	x	Seg.	Seg.

Remark BA: Bank address, Cha.: Channel address, x: High or Low level (Don't care), Seg.: Segment address

This command needs to follow Bank activate (ACT) command. This command fetches data from a segment of the activated row in a bank to a channel buffer which is chosen by channel address. The Segment and Bank fields specify the source segment and bank. In addition, the Channel Address field specifies the destination channel.

A10 specify the optional precharge operation. In case of A10: low, without auto precharge operation occurs. In case of A10: high, with auto precharge operation occurs after data fetch operation. (Please refer to PFCA command.) (Bank precharge is necessary after data fetch.)

This fetched command can be issued continuously without any precharge operation. For instance, when the first operation has been done from one of segment on activated row area to one of channel, if the second prefetch operation is required from same activated row, but different channel, the second prefetch command can be issued without any precharge operation. tPPD (PFC to PFC/PFCA command period) is required between first and second prefetch command. When the new row address area need to be activated on same bank, bank precharge is necessary after this PFC command. tPPL (PFC to PRE command period) is required between PFC and PRE. Fetched data into the channel buffer remains available for Channel Read and Channel Write operations.

Figure 11
Prefetch without Precharge Timing

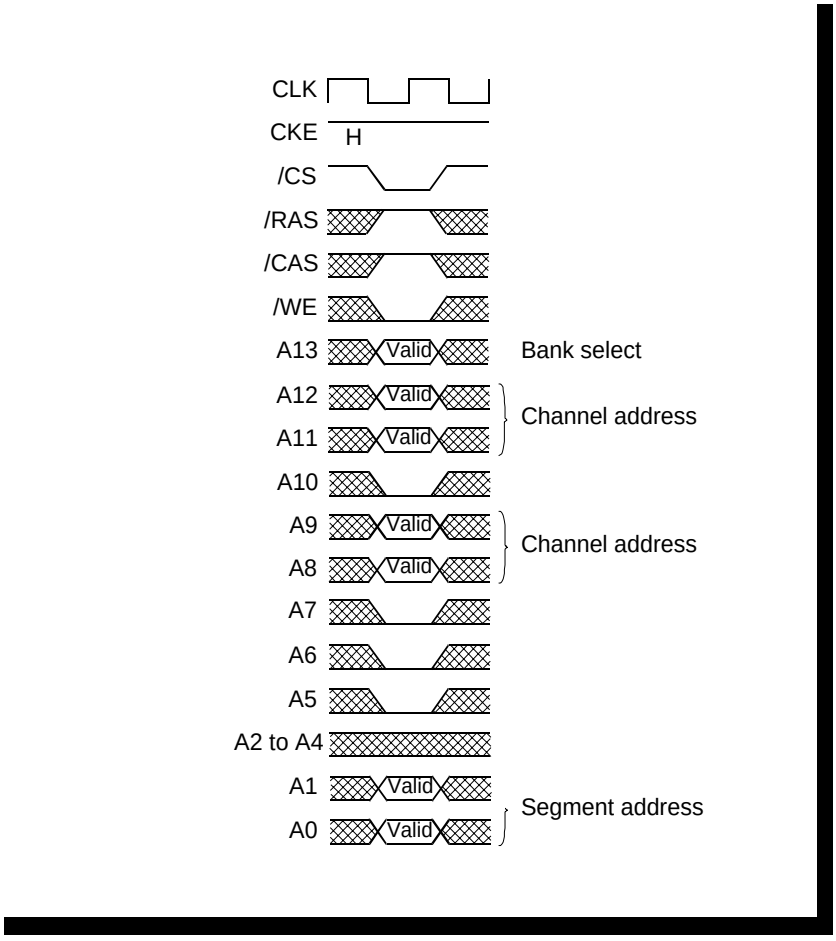


Table 13
Pair Prefetch without Autoprecharge

Pair prefetch without auto precharge (PPF)

/CS	/RAS	/CAS	/WE	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Low	High	High	Low	BA	Cha.	Cha.	Low	Cha.	Cha.	Low	High	x	x	x	x	Seg.	Seg.

Remark BA: Bank address, Cha.: Channel address, x: High or Low level (Don't care), Seg.: Segment address

This command needs to follow Bank activate (ACT) command. This command fetches data from a couple of segments of the activated row in a bank to a couple of channels which are chosen by channel address. (Please refer to Pair Prefetch Operation.) The Segment and Bank fields specify the source segment and bank. In addition, the Channel Address field specifies the destination channel.

A10 specify the optional precharge operation.

In case of A10: low, without auto precharge operation occurs.

In case of A10: high, with auto precharge operation occurs after data fetch operation.

(Please refer to PPFA command.)

Figure 12
Pair Prefetch without Autoprecharge Timing

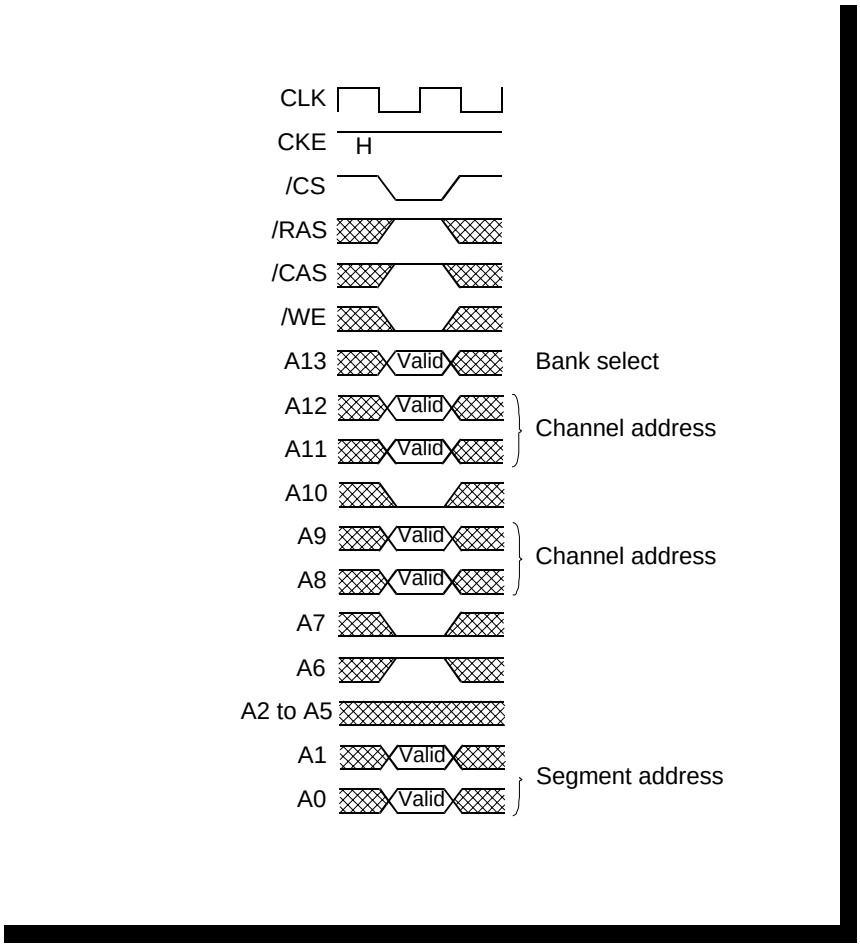


Table 14
Prefetch to Dummy without Autoprecharge Command

Prefetch to dummy without auto precharge (PFD)

/CS	/RAS	/CAS	/WE	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Low	High	High	Low	BA	x	x	x	x	x	Low	Low	High	x	x	x	Seg.	Seg.

Remark BA: Bank address, x: High or Low level (Don' t care), Seg.: Segment address

This command needs to follow Bank activate (ACT) command. This command fetches data from a segment of the activated row in a bank to a dummy channel buffer. The Segment and Bank fields specify the source segment and bank. When this command is input, foreground operation must not be executed.

Figure 13
Prefetch to Dummy without Autoprecharge Timing

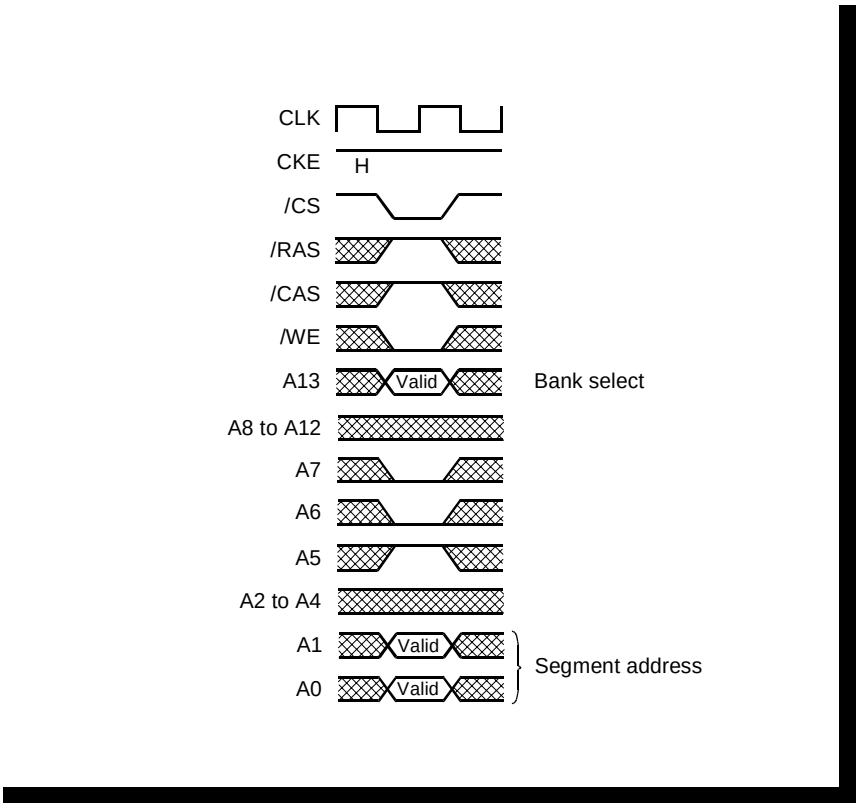


Table 15
Prefetch with Autoprecharge Command

Prefetch with auto precharge (PFCA)

/CS	/RAS	/CAS	/WE	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Low	High	High	Low	BA	Cha.	Cha.	High	Cha.	Cha.	Low	Low	Low	x	x	x	Seg.	Seg.

Remark BA: Bank address, Cha.: Channel address, x: High or Low level (Don't care), Seg.: Segment address

This command needs to follow Bank activate (ACT) command. This command fetches data from a segment of the activated row in a bank to a channel buffer, and precharge operation is performed automatically, which closes the activated row after data fetch operation.

The Segment and Bank fields specify the source segment and bank.

In addition, the Channel Address field specifies the destination channel.

A10 specify the optional precharge operation.

In case of A10: low, without auto precharge operation occurs. (Please refer to PFC command.)

In case of A10: high, with auto precharge operation occurs after data fetch operation.

Fetched data into the channel buffer remains available for Channel Read and Channel Write operations.

Figure 14
Prefetch with Autoprecharge Timing

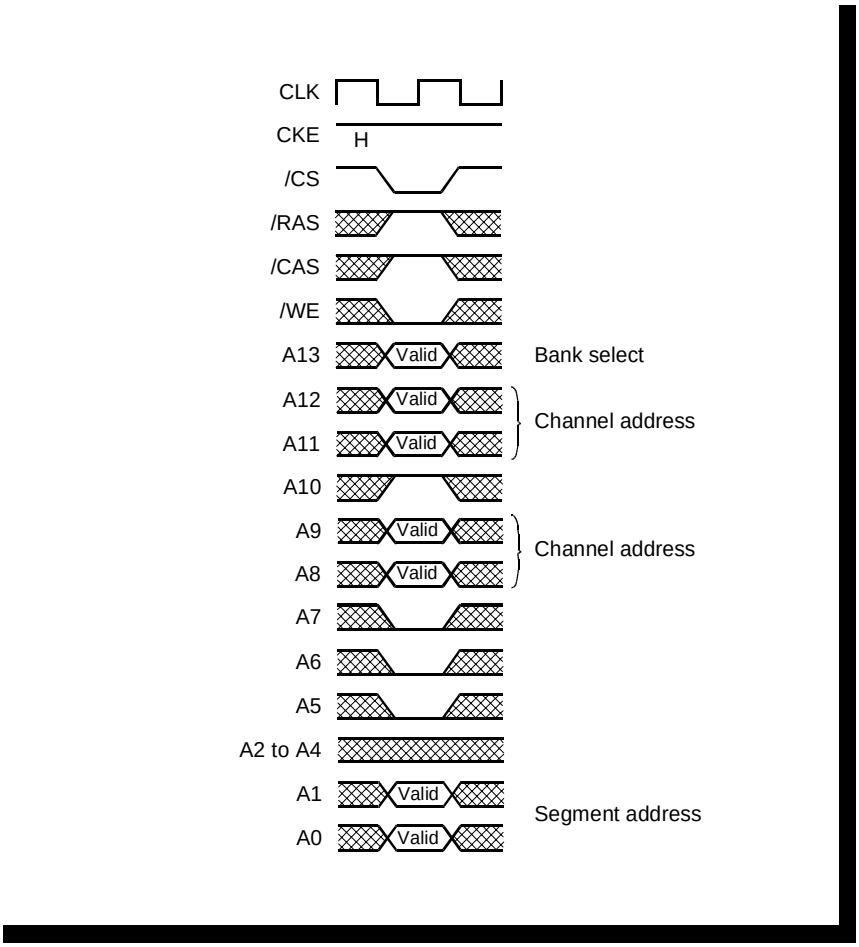


Table 16
Pair Prefetch with Autoprecharge Command

Pair prefetch with auto precharge (PPFA)

/CS	/RAS	/CAS	/WE	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Low	High	High	Low	BA	Cha.	Cha.	High	Cha.	Cha.	Low	High	x	x	x	x	Seg.	Seg.

Remark BA: Bank address, Cha.: Channel address, x: High or Low level (Don't care), Seg.: Segment address

This command needs to follow Bank activate (ACT) command. This command fetches data from a couple of segments of the activated row in a bank to a couple of channels which are chosen by channel address. Precharge operation is performed automatically, which closes the activated row after data fetch operation. (Please refer to Pair Prefetch Operation.) The Segment and Bank fields specify the source segment and bank. In addition, the Channel Address field specifies the destination channel.

A10 specify the optional precharge operation.

In case of A10: low, without auto precharge operation occurs. (Please refer to PPF command.)

In case of A10: high, with auto precharge operation occurs after data fetch operation.

Figure 15
Pair Prefetch with Autoprecharge Timing

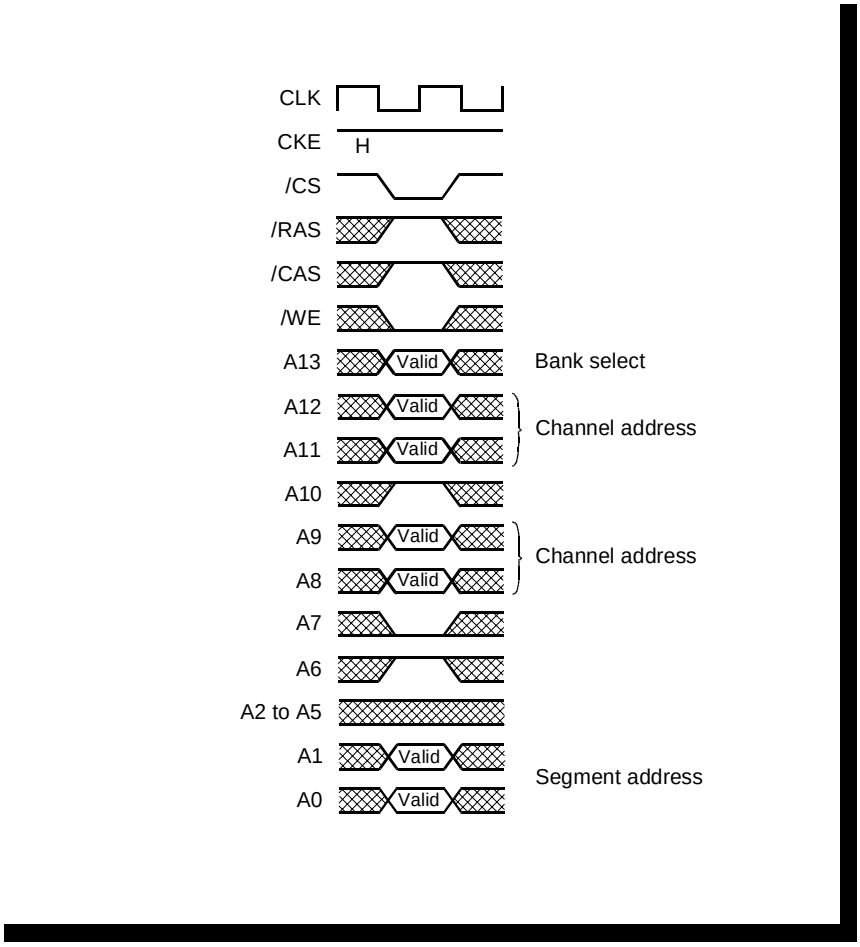


Table 17
Restore without Autoprecharge Command

Restore without auto precharge (RST)

/CS	/RAS	/CAS	/WE	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Low	High	High	Low	BA	Cha.	Cha.	Low	Cha.	Cha.	High	x	x	x	x	x	Seg.	Seg.

Remark BA: Bank address, Cha.: Channel address, x: High or Low level (Don't care), Seg.: Segment address

This command transfers data from a channel buffer to a segment of a row which is going to be activated by following ACT command.
The command Bank Address field specifies the destination bank.
The Channel Address fields specify the source channel.
The Segment number field specifies the destination segment.
A10 specify the optional precharge operation.
In case of A10: low, without auto precharge operation occurs. (Please refer to RSTA command.)
In case of A10: high, with auto precharge operation occurs after data fetch operation.

Figure 16
Restore without Autoprecharge Timing

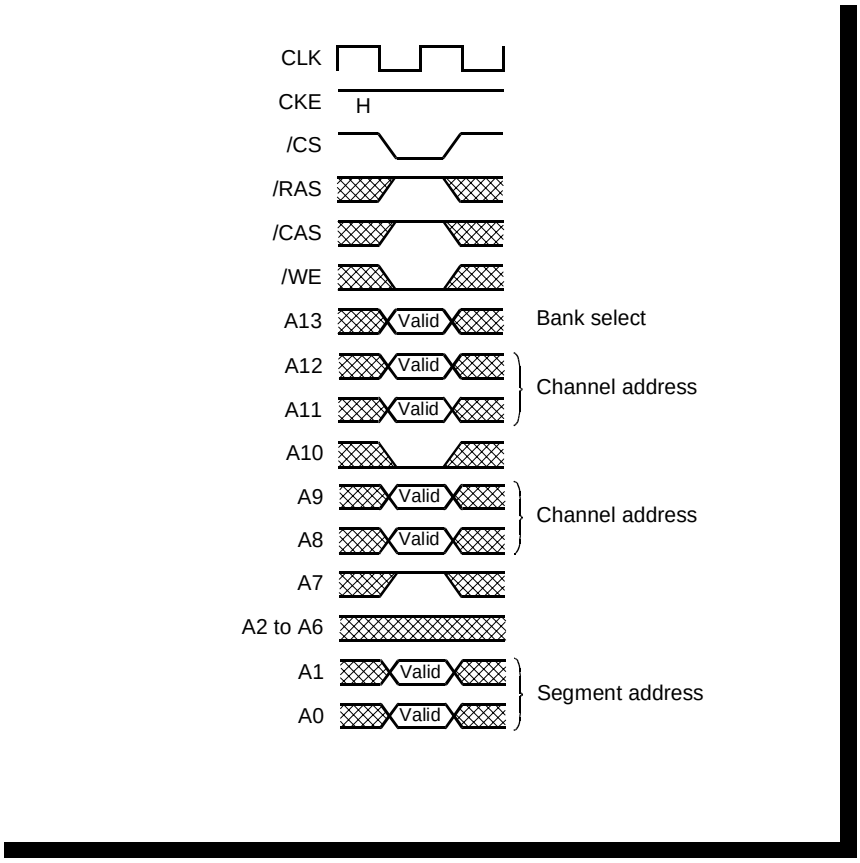


Table 18
Restore with Autoprecharge Command

Restore with auto precharge (RSTA)

/CS	/RAS	/CAS	/WE	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Low	High	High	Low	BA	Cha.	Cha.	High	Cha.	Cha.	High	x	x	x	x	x	Seg.	Seg.

Remark BA: Bank address, Cha.: Channel address, x: High or Low level (Don't care), Seg.: Segment address

This command transfers data from a channel buffer to a segment of a row which is going to be activated by following ACT command.
In addition, precharge operation is performed automatically which closes the active row after data restore operation.
The command Bank Address field specifies the destination bank.
The Channel Address fields specify the source channel.
The Segment number field specifies the destination segment.
A10 specify the optional precharge operation.
In case of A10: low, without auto precharge operation occurs. (Please refer to RSTA command.)
In case of A10: high, with auto precharge operation occurs after data fetch operation.

Figure 17
Restore with Autoprecharge Timing

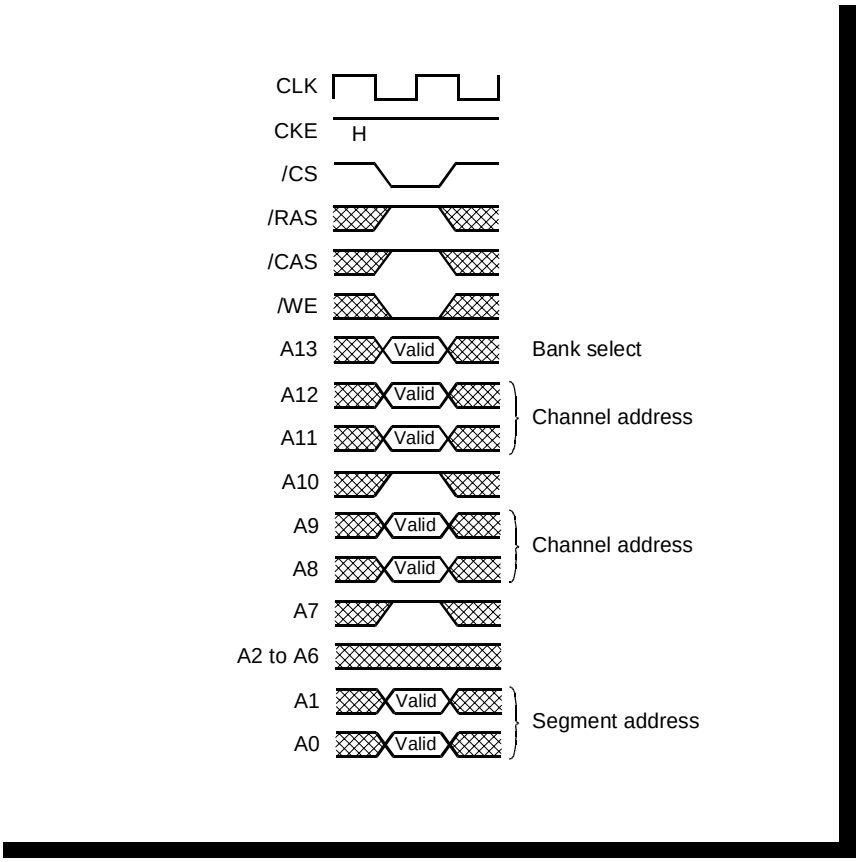


Table 19
Channel Read Command

Channel read (READ)

/CS	/RAS	/CAS	/WE	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Low	High	Low	High	x	Cha.	Cha.	x	Cha.	Cha.	Col.	Col.	Col.	Col.	Col.	Col.	Col.	Col.

Remark x: High or Low level (Don't care), Cha.: Channel address, Col.: Column address

Channel Read (READ) reads data words from a channel buffer onto the data bus (DQ). The Channel Address field specifies the source channel. The Column Address field specifies the starting location of the data word in the buffer (Data words may be 4, 8, or 16 bits.). The burst-length field in the channel control register for the channel specifies the number of data words to complete the read operation.

Figure 18
Channel Read Timing

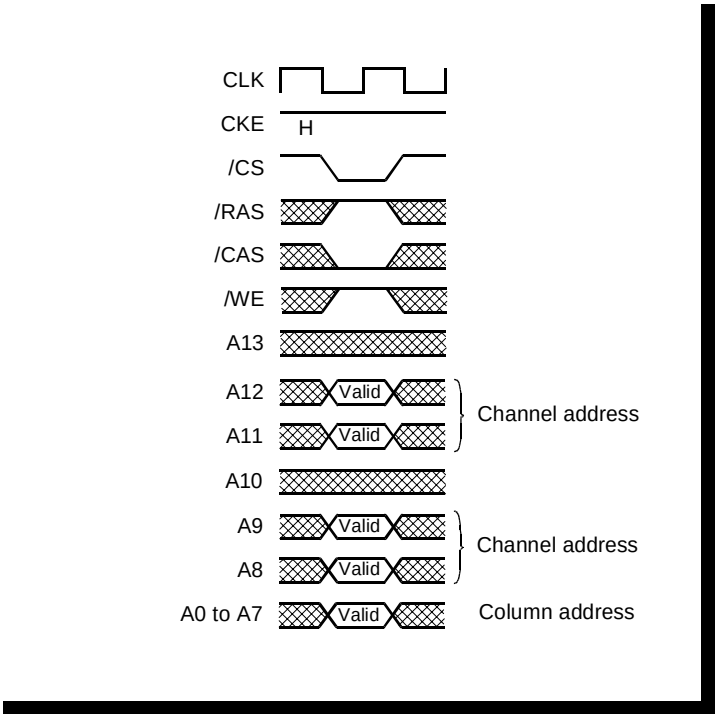


Table 20
Channel Write Command

Channel write (WRIT)

/CS	/RAS	/CAS	/WE	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Low	High	Low	Low	Low	Cha.	Cha.	x	Cha.	Cha.	Col.	Col.	Col.	Col.	Col.	Col.	Col.	Col.

Remark x: High or Low level (Don't care), Cha.: Channel address, Col.: Column address

Channel Write(WRIT) writes data from the data bus (DQ) into a channel buffer. The Channel Address field specifies the destination channel. The Column Address field specifies the starting location of the data word in the buffer (Data words may be 4, 8 or 16 bits.).

The burst-length field in the channel control register for the channel specifies the number of data words to complete the write operation.

Figure 19
Channel Write Timing

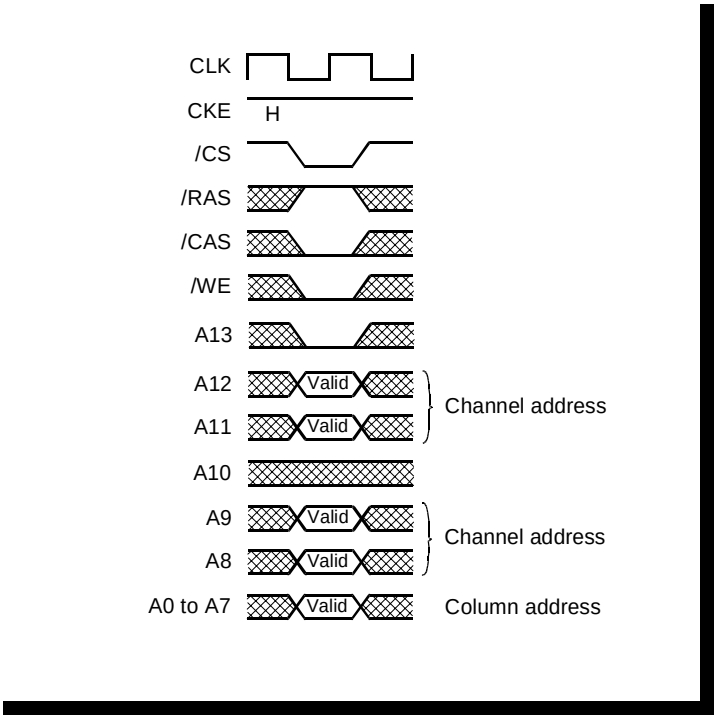


Table 21
Dummy Channel Write without Restore Command

Dummy channel write without auto restore (WRD)

/CS	/RAS	/CAS	/WE	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Low	High	Low	Low	High	x	x	x	x	Low	Col.	Col.	Col.	Col.	Col.	Col.	Col.	Col.

Remark x: High or Low level (Don't care), Col.: Column address

Dummy Channel Write writes data from the data bus (DQ) into a dummy channel buffer. The Column Address field specifies the starting location of the data word in the buffer (Data words may be 4, 8 or 16 bits.).

The burst-length field in the channel control register for the channel specifies the number of data words to complete the write.

A8 specify the optional restore operation.

In case of A8: low, without auto restore operation occurs.

In case of A8: high, with auto restore operation occurs after data fetch operation. (Please refer to WRDA command.)

Figure 20
Dummy Channel Write without Restore Timing

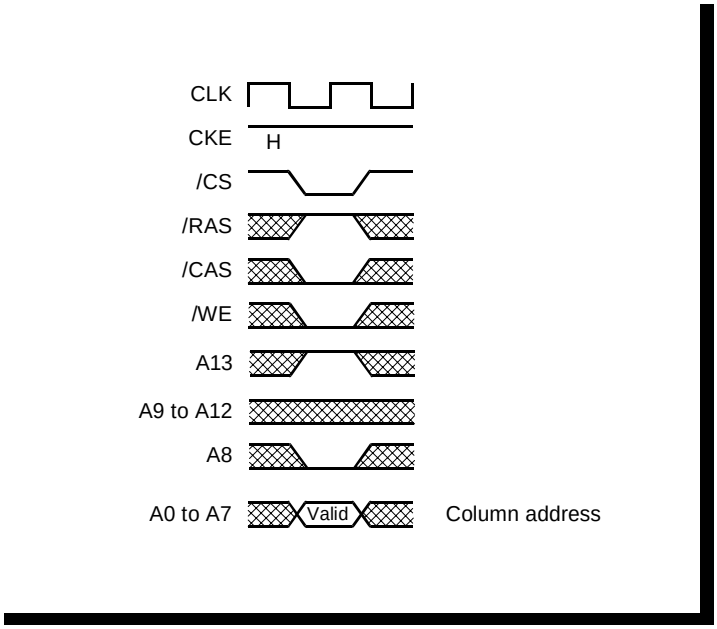


Table 22
Dummy Channel Write with Autorestore

Dummy channel write with auto restore (WRDA)

/CS	/RAS	/CAS	/WE	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Low	High	Low	Low	High	x	x	x	x	High	Col.	Col.	Col.	Col.	Col.	Col.	Col.	Col.

Remark x: High or Low level (Don't care), Col.: Column address

Dummy channel write with auto restore writes data from the data bus (DQ) into a dummy channel buffer. In addition, this command transfers data from a dummy channel buffer to a segment of a row which has been activated by ACT command before this WRDA command. Moreover, precharge operation is performed automatically which closes the active row after data restore operation. The Column Address field specifies the starting location of the data word in the buffer (Data words may be 4, 8 or 16 bits.). The burst-length field in the channel control register for the channel specifies the number of data words to complete the write. (Please refer to WRD command.)

A8 specify the optional restore operation.

In case of A8: low, without auto restore operation occurs. (Please refer to WRD command.)

In case of A8: high, with auto restore operation occurs after data fetch operation.

Figure 21
Dummy Channel Write with Autorestore Timing

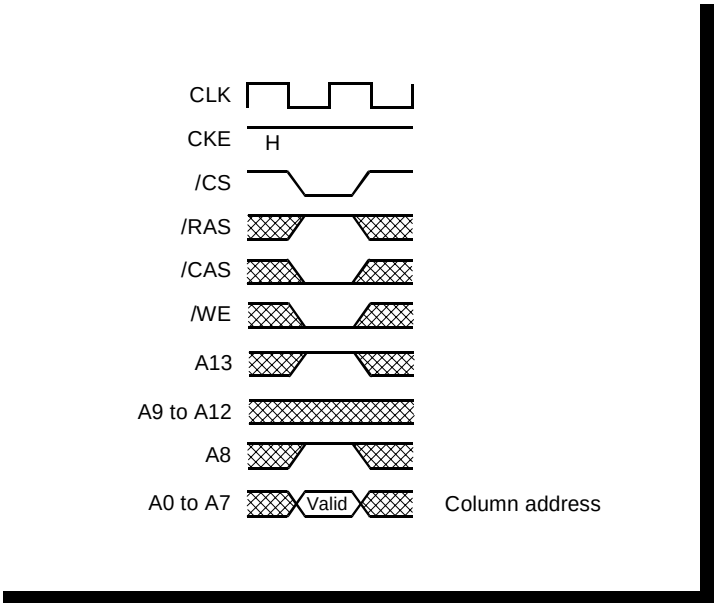


Table 23
Bank Activate Command

Bank activate (ACT)

/CS	/RAS	/CAS	/WE	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Low	Low	High	High	BA	Row	Row	Row	Row	Row	Row	Row	Row	Row	Row	Row	Row	Row

Remark BA: Bank address, Row: Row address

Activation causes row contents to be placed into the bank's sense amplifier. The command Bank Address and Row Address fields specify bank and row. This device has two banks, each with 8,192 rows. This command activates the bank selected by bank address(A13) and a row address selected by A0 through A12. The row remains active for access until a Precharge command is issued to the bank. A Precharge command must be issued before another row can be activated in that bank. Each bank can have one row active. This command corresponds to a conventional DRAM's /RAS falling.

Figure 22
Bank Avtivate Timing

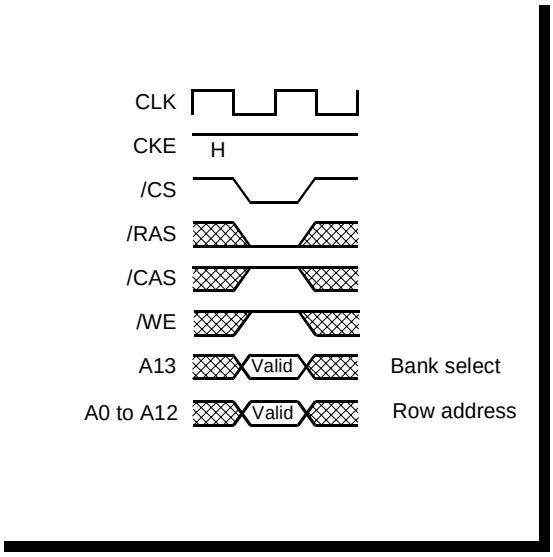


Table 24
Prefetch Read with Autoprecharge Command

Prefetch read with auto precharge (PFR)

/CS	/RAS	/CAS	/WE	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Low	Low	High	Low	Seg.	Cha.	Cha.	Seg.	Cha.	Cha.	Col.	Col.	Col.	Col.	Col.	Col.	Col.	Col.

Remark Seg.: Segment address, Cha.: Channel address, Col.: Column address

This command needs to follow Bank activate (ACT) command. This command fetches data from a segment of the activated row in a bank to a channel buffer, and reads data words from a channel buffer onto the data bus (DQ).

In addition, precharge operation is performed automatically, which closes the activated row after data fetch operation.

The Segment fields specify the source segment. In addition, the Channel Address field specifies the destination channel.

The Column Address field specifies the starting location of the data word in the buffer (Data words may be 4, 8, or 16 bits.). The burst-length field in the channel control register for the channel specifies the number of data words to complete the read operation.

Figure 23
Prefetch Read with Autoprecharge Timing

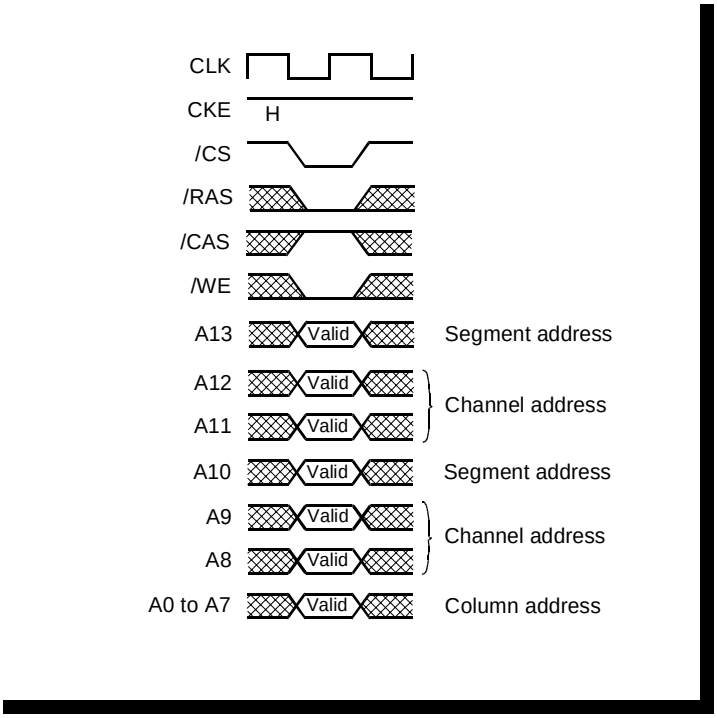


Table 25
Precharge Selected Bank Command

Precharge selected bank (PRE)

/CS	/RAS	/CAS	/WE	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Low	Low	Low	Low	BA	x	x	Low	x	x	x	x	Low	x	x	x	x	x

Remark BA: Bank address, x: High or Low level (Don't care)

This command closes (deactivates) an activated row in a bank, in order to prepare the bank for an Activate or Restore command to activate a new row. After precharging, a bank is in the Idle state.

The Bank field specifies the bank to precharge and A10 Low specifies the command.

After this command, tRP (precharge to activate command period) must be satisfied for next activate command to precharging bank.

This command corresponds to a conventional DRAM's /RAS rising.

Figure 24
Precharge Selected Bank Timing

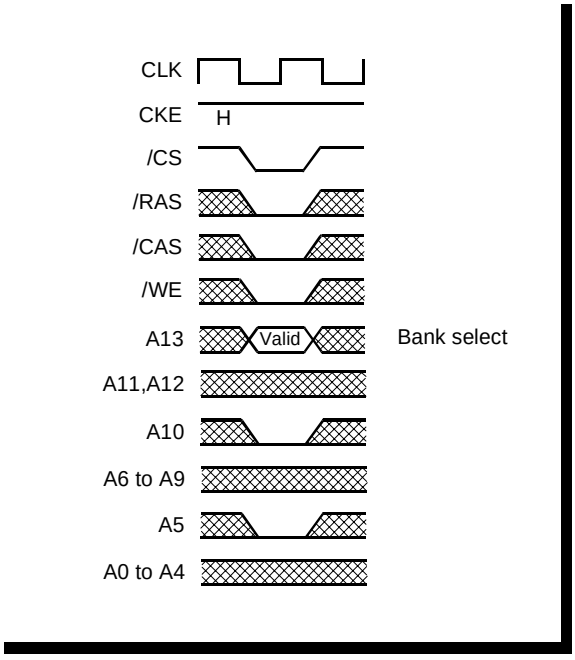


Table 26
Precharge All Banks Command

Precharge all banks (PALL)

/CS	/RAS	/CAS	/WE	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Low	Low	Low	Low	x	x	x	High	x	x	x	x	Low	x	x	x	x	x

Remark x: High or Low level (Don't care)

The signal combination is Reserved (with command modifier A10 High). The PALL command is typically used during auto refresh operation and initialization. Replace with Precharge commands for each bank.

Figure 25
Precharge All Banks Timing

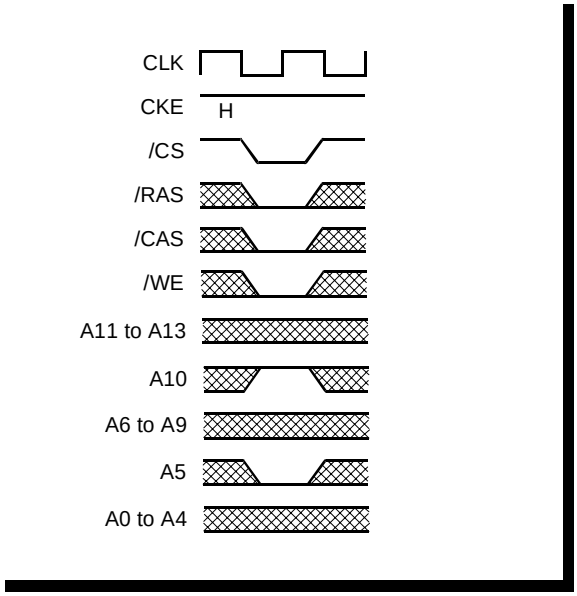


Table 27
Set Channel Latency Register Command

Set Channel Latency Register (SCLR)

/CS	/RAS	/CAS	/WE	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	High	PRL	RL	RL	RL	WT

Remark PRL: Prefetch Read Latency, RL: Read Latency, WT: Wrap Type

This command sets the Read Latency value which specifies read delay time in channel read operation.

In addition, this command sets the Wrap type which specifies the order(Sequential or Interleave) in which the burst data will be addressed.

Moreover, this command sets the Read Latency value which specifies read delay time in prefetch read operation.

The commands can only be executed with all memory banks idle and no burst operations in progress.

Figure 26
Set Channel Latency Register Timing

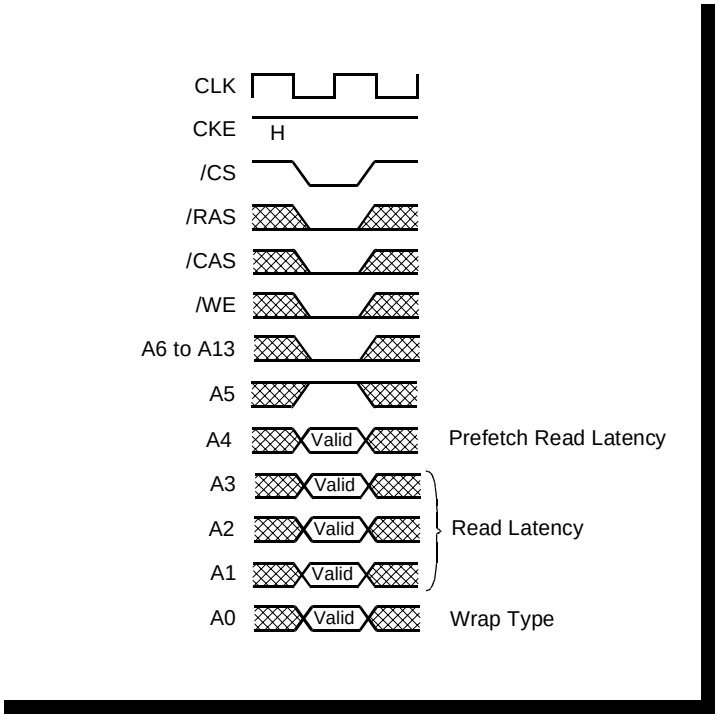


Table 28
Set Channel Control Register Command

Set Channel Control Register (SCCR)

/CS	/RAS	/CAS	/WE	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Low	Low	Low	Low	Cha.	Cha.	Cha.	Cha.	Cha.	Low	Low	High	High	x	x	BL	BL	BL

Remark Cha.: Channel address, BL: Burst Length, x: High or Low level (Don't care)

This command sets Burst Length in channel address.

Burst Length for the 0-15 channels is the same. However, another burst length can be set for the dummy channel.

This command is executed during Initialization.

The commands can only be executed with all memory banks idle and no burst operations in progress.

To set the burst length in dummy channel address, A13: high, the other channel address: do not care.

Figure 27
Set Channel Control Register Timing

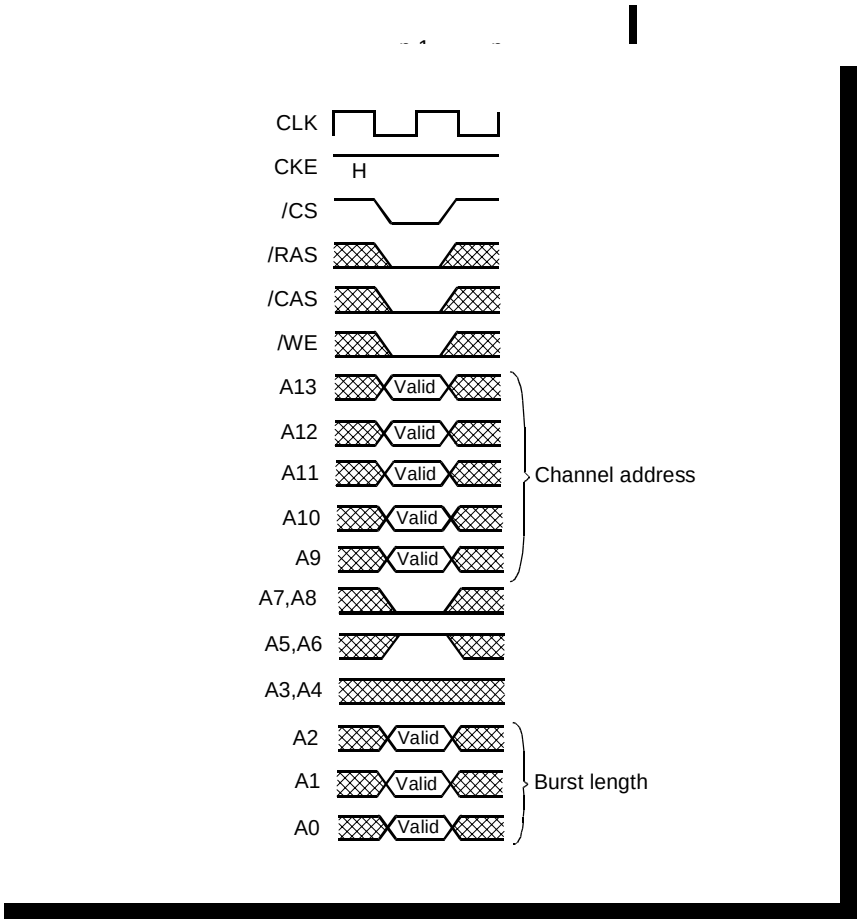


Table 29
Auto Refresh Command

Auto Refresh (REF)

	CKE		*/CS*	*/RAS*	*/CAS*	*/WE*	*Address*
	n–1	*n*					
	High	High	Low	Low	Low	High	High or Low level (Don't care)

This command is a request to begin the auto refresh operation. The refresh address is generated internally.

Before executing auto refresh, all banks must be in the idle state. After this cycle, all banks will be in the idle (precharged) state and ready for a row activate command. During tRC period (from refresh command to refresh or activate command), the VC SDRAM cannot accept any other command.

Figure 28
Auto Refresh Timing

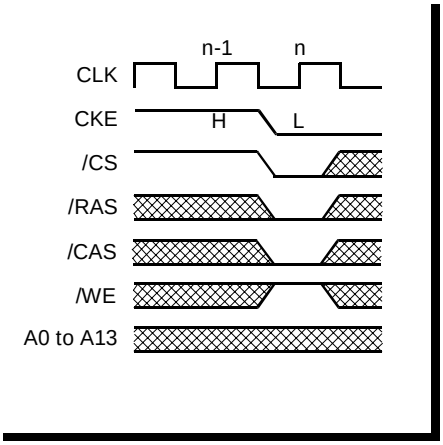


Table 30
Self Refresh Command

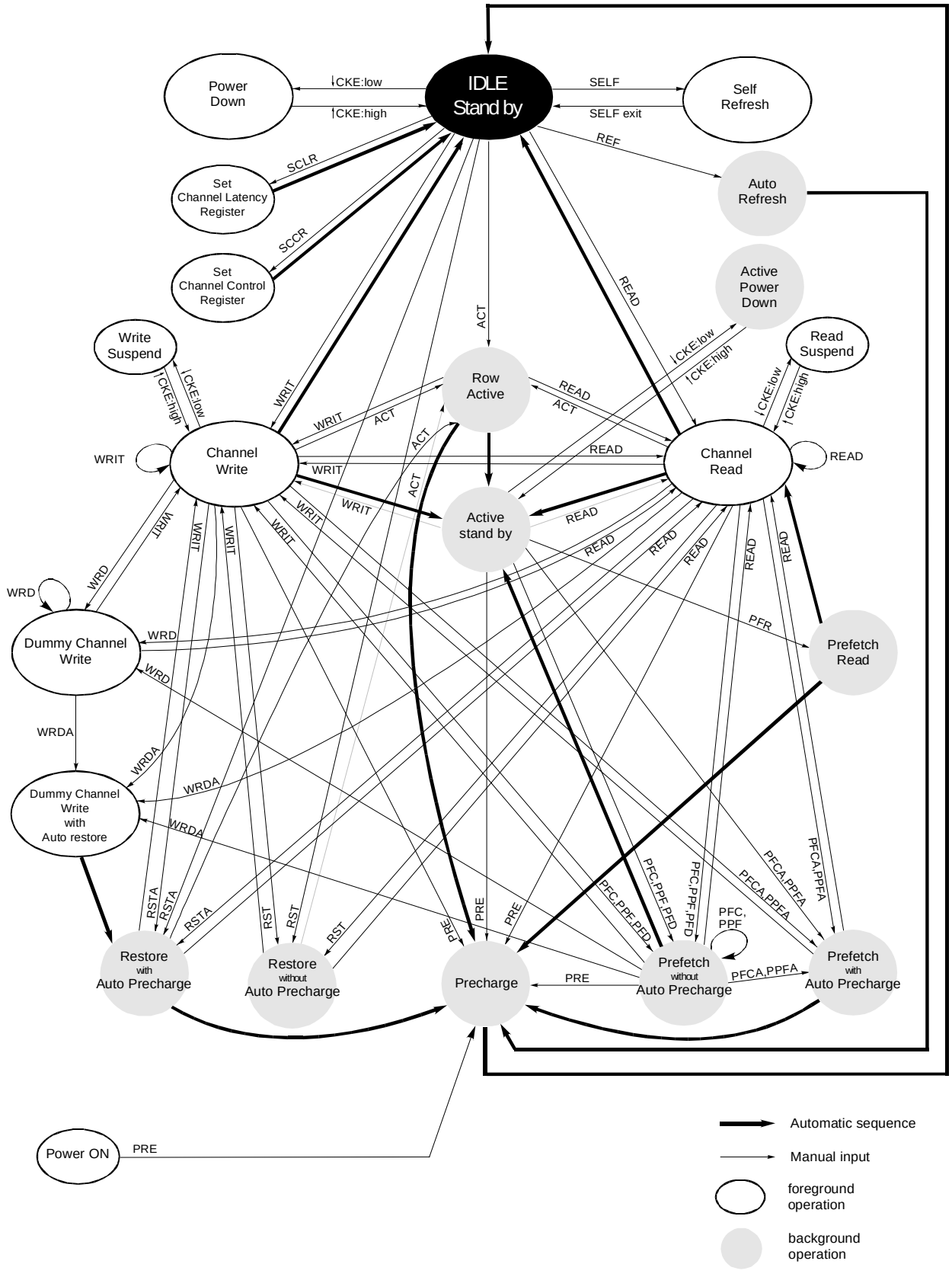
	CKE n-1	CKE n	/CS	/RAS	/CAS	/WE	Address
Self Refresh (SELF)	High	Low	Low	Low	Low	High	High or Low level (Don't care)

After the command execution, self refresh operation continues while CKE remains low. During self refresh mode, the internal refresh controller takes care of refresh interval and refresh operation. There is no need for external control. Before executing self refresh, both banks must be in the idle state.

Figure 29
Self Refresh Timing

2.7 State Diagram

Figure 30
Simplified State Diagram



2.8 Prefetch Read Operation (Optional)

This operation fetches data from a segment of the activated row in a bank to a channel buffer, and reads data words from a channel buffer onto the data bus (DQ). In addition, precharge operation is performed automatically, which closes the activated row after data fetch operation.

Figure 31
Prefetch Read Operation Basics

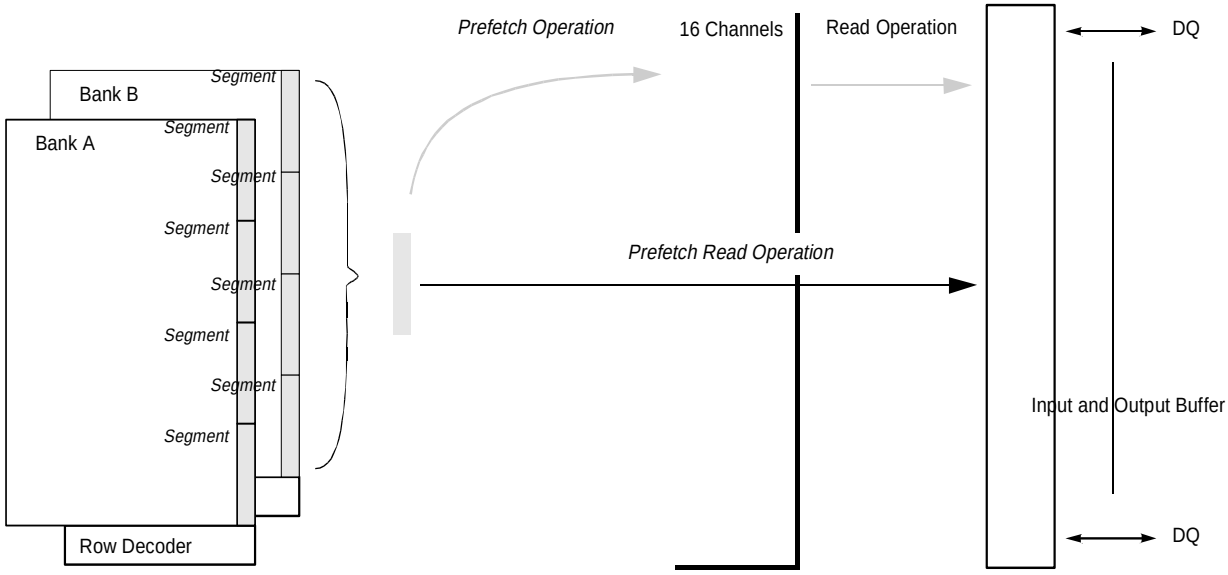
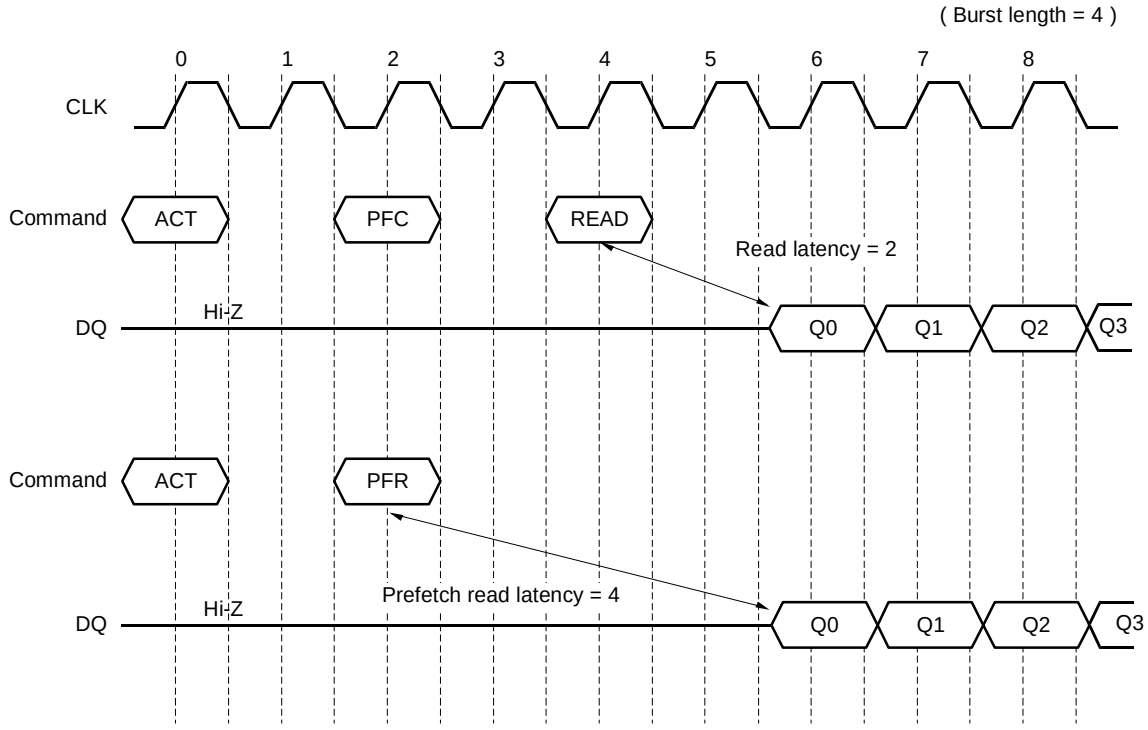


Figure 32
Prefetch Read Operation Timing



2.9 Write Operation and Restore Operation

Write command proceeds write operation to the channel. When the system needs to refill the channel with new data, restore operation may be necessary. The restore operation needs both restore command and active command. Restore command must be first command. Restore operation is also fully associative operation.
The data in the channel can be transferred to anywhere on memory core array. Another write and read operation to another channel can proceed during this restore operation.
The another background operation is illegal while tRAD (RST/RSTA to ACT(R) command delay time). In addition, the foreground operation to the same channel set by RST command is illegal too.

Figure 33
Write and Restore Operation Basics

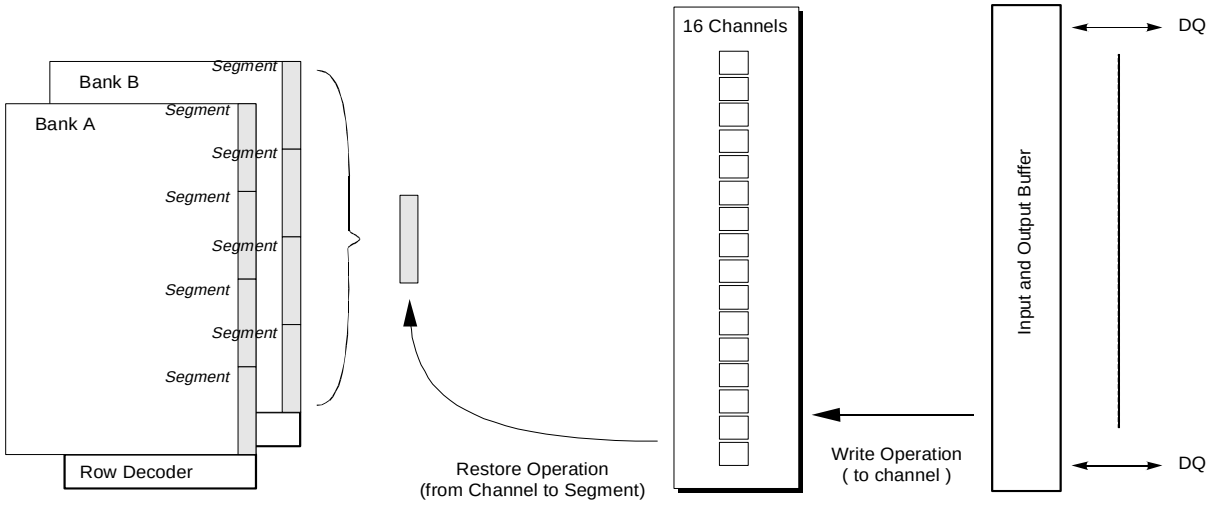
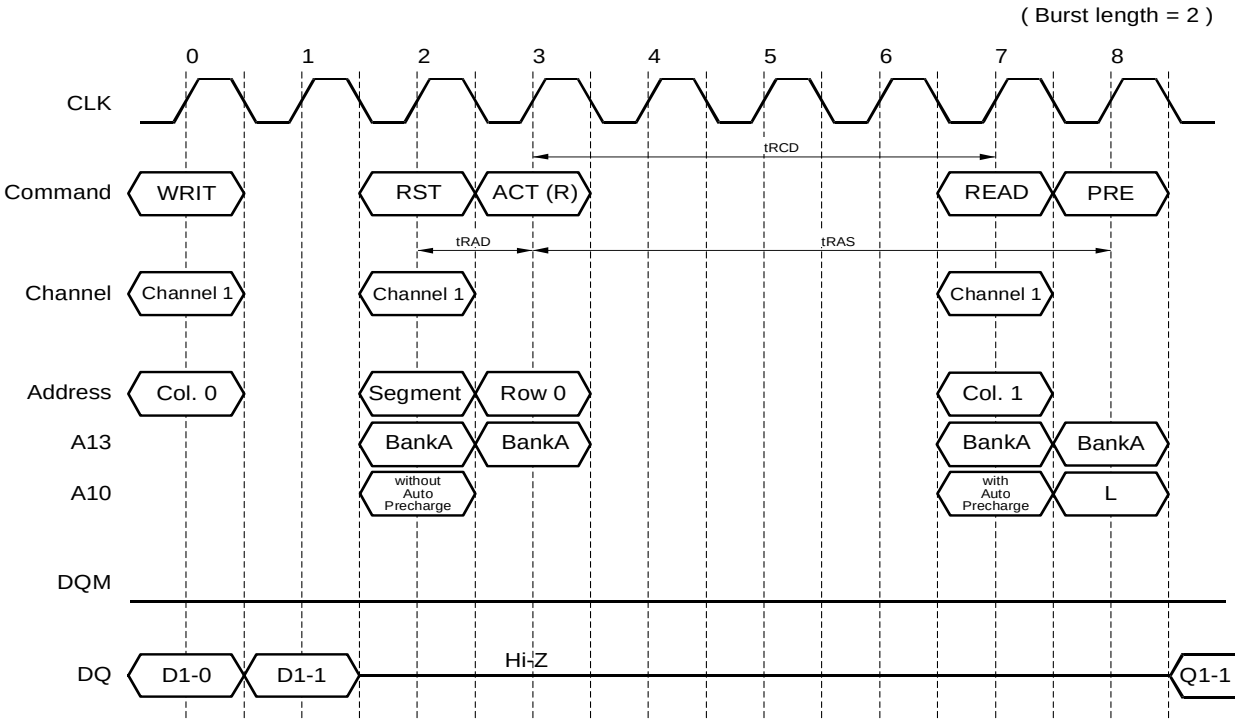


Figure 34
Write and Restore Operation Timing



Remark ACT(R) command is ACT command after RST command.

2.10 Dummy Channel

This device has actually seventeen channels. The 17th channel is dummy channel for direct write operation to the array. The operations for dummy channel are as follows.

Prefetching to Dummy channel

Writing to Dummy channel

Writing to Dummy channel with Auto Restore

Dummy channel write with auto restore writes data from the data bus (DQ) into a Dummy channel buffer, and transfers the data from a dummy channel buffer to a segment of a row which has been activated by ACT command before this WRDA command. It is impossible to read from Dummy channel. In addition, it needs prefetch operation to the Dummy channel before write to the Dummy operation.

To execute the background operation, it is necessary to complete the write operation to the dummy channel.

Moreover, the write operation to the dummy channel is completed by WRDA command.

Figure 35
Dummy Channel Basics

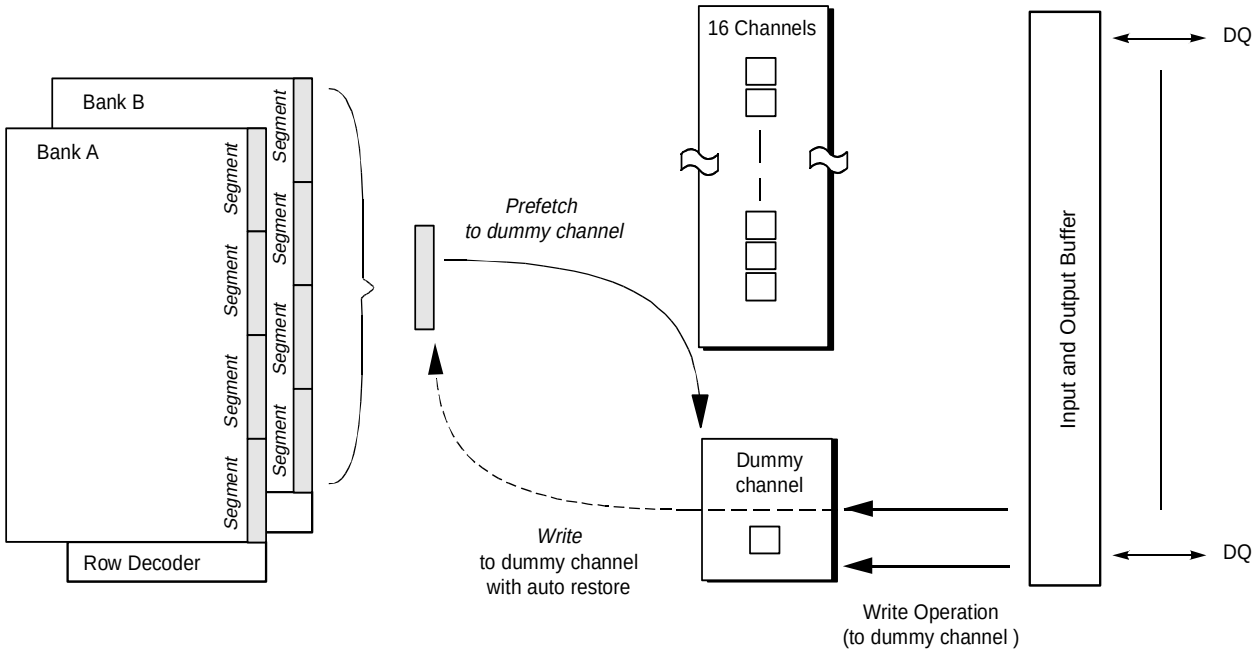
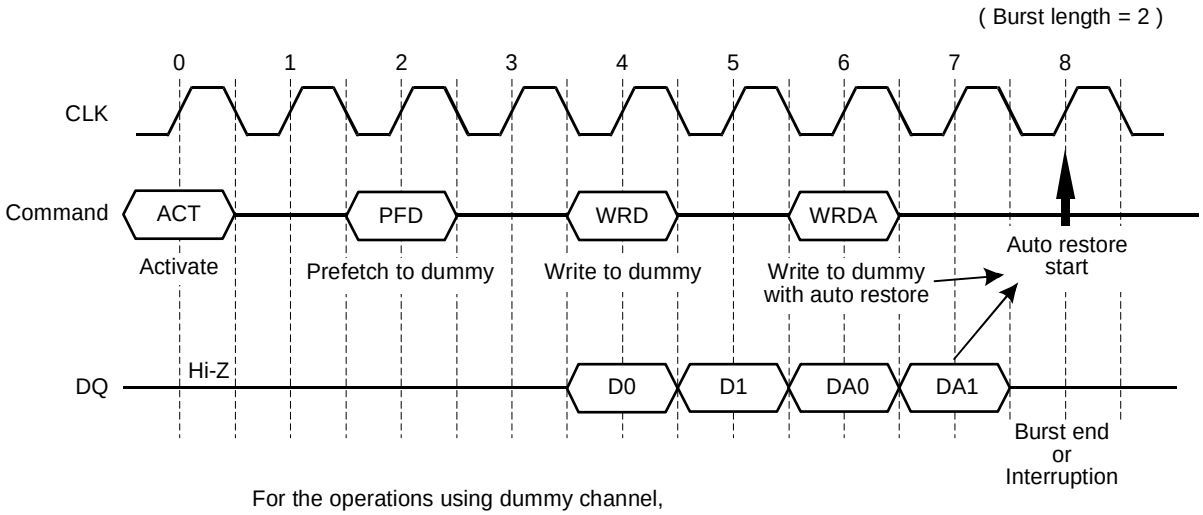


Figure 36
Dummy Channel Write Timing Diagram



For the operations using dummy channel,
it needs PFD command(prefetch to dummy) after ACT command.

2.11 Pair Prefetch Operation

Pair prefetch operation fetches data from a couple of segments to a couple of channels at one operations. In this operation, four segments are devided to two segment pairs and sixteen channels are devided to eight channels pairs.

Each pair of segments and channels consists of odd address and even address. In addition, prefetch operation is from even segment to even channel and from odd segment to odd channel. If the even segment is selected at command input, the first prefetch operation starts from even segment to even channel. Moreover, if the odd segment is selected at command input, the first prefetch operation starts from odd segment to odd channel.

The Segment and bank fields specify the source segment and bank. In addition, the Channel Address field specifies the destination channel.

Figure 37
Pair Prefetch Operation Basics 1

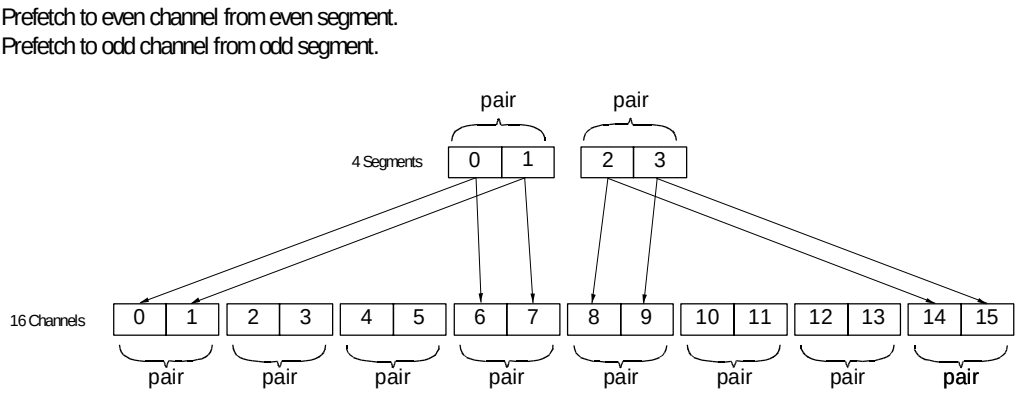
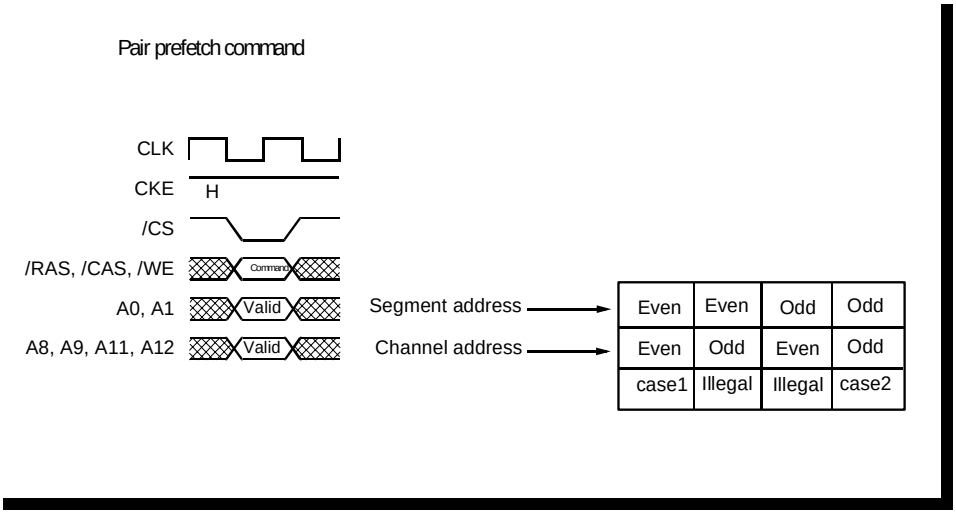
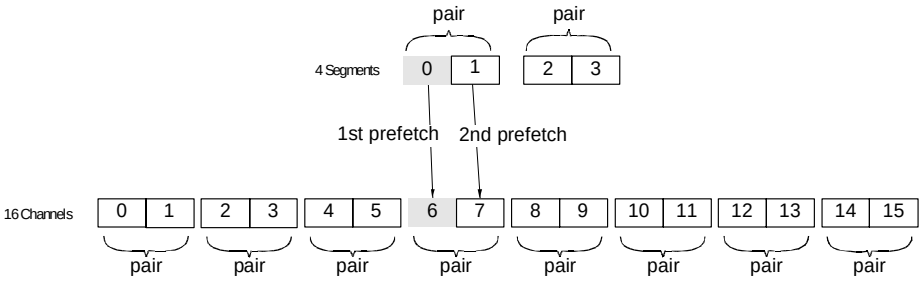


Figure 38
Pair Prefetch Operation Basics 2



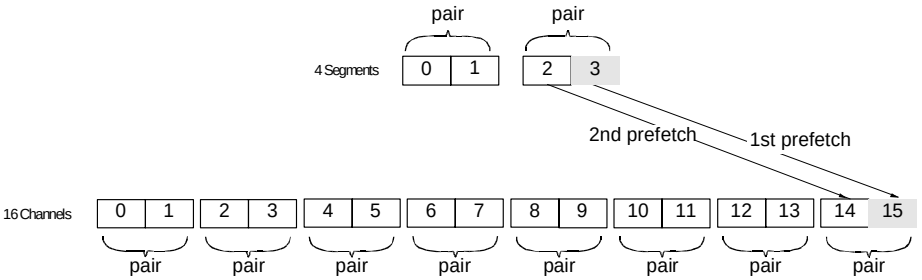
Case1. Segment=Even(0) and Channel=Even(6)

1st Prefetch operation is from even segment to even channel
2nd Prefetch operation is from odd segment to odd channel



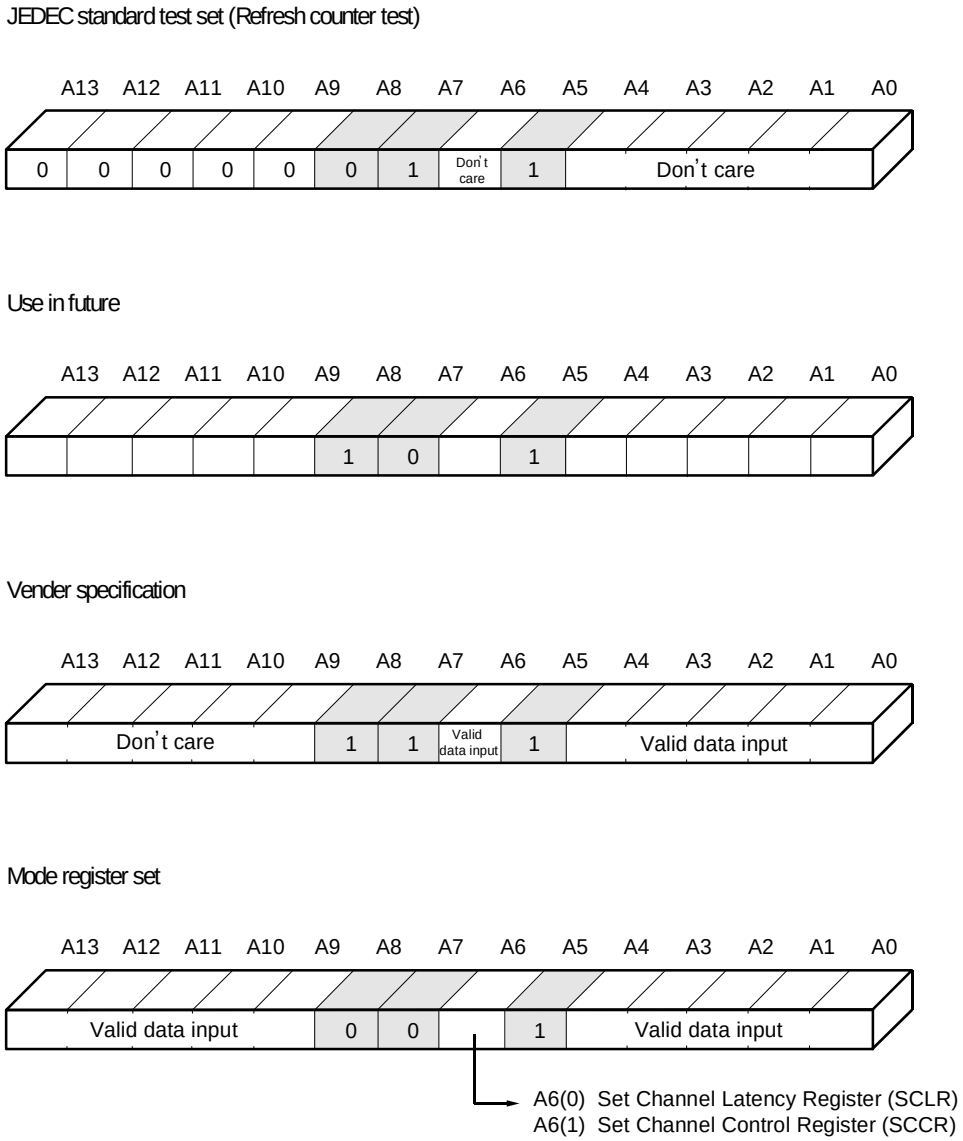
Case2. Segment=Odd(3) and Channel=Odd(15)

1st Prefetch operation is from odd segment to odd channel
2nd Prefetch operation is from even segment to even channel



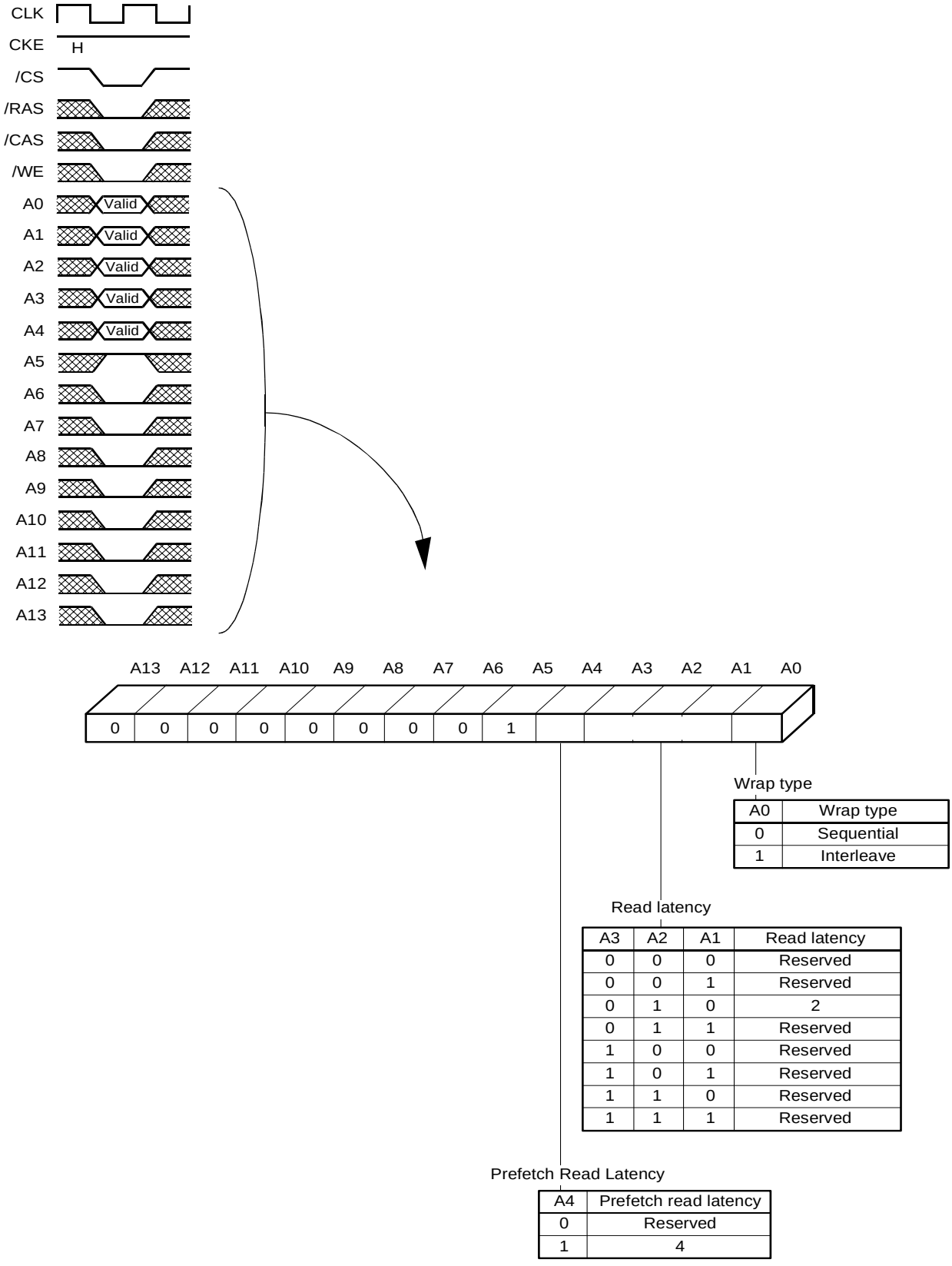
2.12 Set Register Operation

Figure 39
Register Set Overview



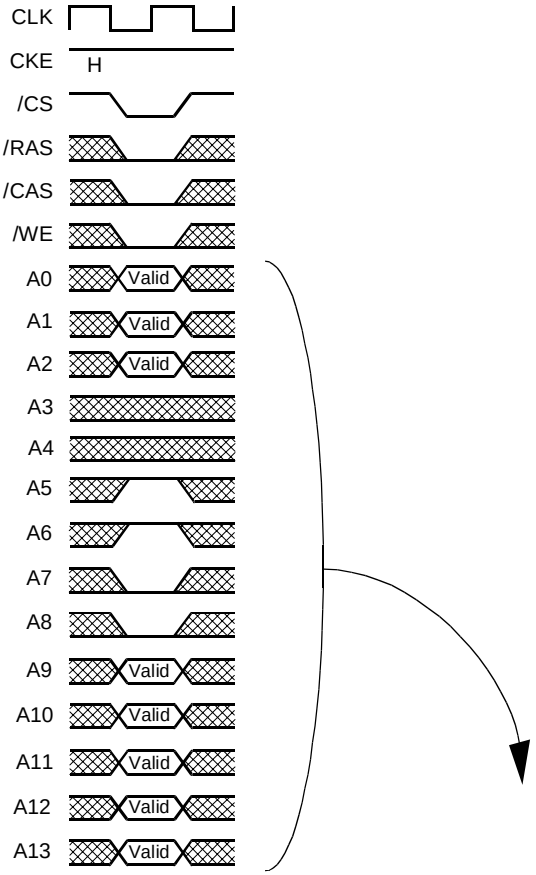
2.13 Set Channel Latency Register

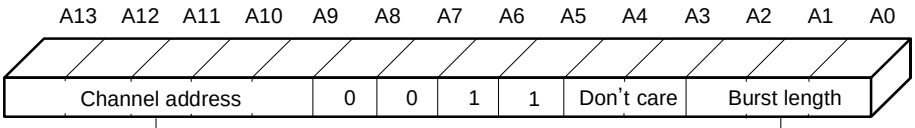
Figure 40
Channel Latency register



2.14 Set Channel Control Register

Figure 41
Channel Control Register





Channel number

Channel number	A13	A12	A11	A10	A9
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
3	0	0	0	1	1
4	0	0	1	0	0
5	0	0	1	0	1
6	0	0	1	1	0
7	0	0	1	1	1
8	0	1	0	0	0
9	0	1	0	0	1
10	0	1	0	1	0
11	0	1	0	1	1
12	0	1	1	0	0
13	0	1	1	0	1
14	0	1	1	1	0
15	0	1	1	1	1
16 (Dummy)	1	Don't care			

Burst length

Sequential	Interleave	A2	A1	A0
1	1	0	0	0
2	2	0	0	1
4	4	0	1	0
8	8	0	1	1
16	16	1	0	0
Reserved	Reserved	1	0	1
Reserved	Reserved	1	1	0
Reserved	Reserved	1	1	1

2.15 Burst Length and Sequence

Table 31
Overview Burst Lengt and Sequencies of 2, 4, 8

[Burst of Two]

Starting Address (column address A0) (binary)	Addressing Sequence Sequential (decimal)	Addressing Sequence Interleave (decimal)
0	0, 1	0, 1
1	1, 0	1, 0

[Burst of Four]

Starting Address (column address A1,A0) (binary)	Addressing Sequence Sequential (decimal)	Addressing Sequence Interleave (decimal)
00	0, 1, 2, 3	0, 1, 2, 3
01	1, 2, 3, 0	1, 0, 3, 2
10	2, 3, 0, 1	2, 3, 0, 1
11	3, 0, 1, 2	3, 2, 1, 0

[Burst of Eight]

Starting Address (column address A2-A0) (binary)	Addressing Sequence Sequential (decimal)	Addressing Sequence Interleave (decimal)
000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
011	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
101	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
110	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
111	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

Table 32
Burst Length and Sequencies of 16

[Burst of Sixteen]

Starting Address (column address A3-A0) (binary)	Addressing Sequence Sequential (decimal)	Addressing Sequence Interleave (decimal)
0000	0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15	0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15
0001	1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,0	1,0,3,2,5,4,7,6,9,8,11,10,13,12,15,14
0010	2,3,4,5,6,7,8,9,10,11,12,13,14,15,0,1	2,3,0,1,6,7,4,5,10,11,8,9,14,15,12,13
0011	3,4,5,6,7,8,9,10,11,12,13,14,15,0,1,2	3,2,1,0,7,6,5,4,11,10,9,8,15,14,13,12
0100	4,5,6,7,8,9,10,11,12,13,14,15,0,1,2,3	4,5,6,7,0,1,2,3,12,13,14,15,8,9,10,11
0101	5,6,7,8,9,10,11,12,13,14,15,0,1,2,3,4	5,4,7,6,1,0,3,2,13,12,15,14,9,8,11,10
0110	6,7,8,9,10,11,12,13,14,15,0,1,2,3,4,5	6,7,4,5,2,3,0,1,14,15,12,13,10,11,8,9
0111	7,8,9,10,11,12,13,14,15,0,1,2,3,4,5,6	7,6,5,4,3,2,1,0,15,14,13,12,11,10,9,8
1000	8,9,10,11,12,13,14,15,0,1,2,3,4,5,6,7	8,9,10,11,12,13,14,15,0,1,2,3,4,5,6,7
1001	9,10,11,12,13,14,15,0,1,2,3,4,5,6,7,8	9,8,11,10,13,12,15,14,1,0,3,2,5,4,7,6
1010	10,11,12,13,14,15,0,1,2,3,4,5,6,7,8,9	10,11,8,9,14,15,12,13,2,3,0,1,6,7,4,5
1011	11,12,13,14,15,0,1,2,3,4,5,6,7,8,9,10	11,10,9,8,15,14,13,12,3,2,1,0,7,6,5,4
1100	12,13,14,15,0,1,2,3,4,5,6,7,8,9,10,11	12,13,14,15,8,9,10,11,4,5,6,7,0,1,2,3
1101	13,14,15,0,1,2,3,4,5,6,7,8,9,10,11,12	13,12,15,14,9,8,11,10,5,4,7,6,1,0,3,2
1110	14,15,0,1,2,3,4,5,6,7,8,9,10,11,12,13	14,15,12,13,10,11,8,9,6,7,4,5,2,3,0,1
1111	15,0,1,2,3,4,5,6,7,8,9,10,11,12,13,14	15,14,13,12,11,10,9,8,7,6,5,4,3,2,1,0

2.16 Initialization

The VC SDRAM is initialized according to the following power-on sequence.

1. To stabilize internal circuits, when power is applied, a 100 ms or longer pause must precede any signal toggling.
2. After the pause, both banks must be precharged using the Precharge command (The Precharge all banks command is convenient).
3. Once the precharge is completed and the minimum tRP is satisfied, the mode register can be programmed. After the mode register set cycle, t_{RSC} (2 CLK minimum) pause must be satisfied as well.
4. Two or more auto refresh must be performed.

Note: 1. The sequence of Mode register programming and Refresh above may be transposed.
2. CKE and DQM must be held high until the Precharge command is issued to ensure data-bus Hi-Z.

3 Specifications

3.1 DC Electrical Specifications

- All voltages are referenced to VSS (GND).
- After power up, wait more than 100 ms and then, execute Power on sequence and Auto Refresh before proper device operation is achieved.

Table 33
Absolut Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on power supply pin relative to GND	VCC, VCCQ		–0.5 to +4.6	V
Voltage on input pin relative to GND	VT		–0.5 to +4.6	V
Short circuit output current	IO		50	mA
Power dissipation	PD		1	W
Operating ambient temperature	TA		0 to +70	°C
Storage temperature	Tstg		–55 to +125	°C

Note: ***Caution!***
Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 34
Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	VCC, VCCQ		3.0	3.3	3.6	V
High level input voltage	VIH		2.0		VCC + 0.3	V
Low level input voltage	VIL		–0.3		0.8	V
Operating ambient temperature	TA		0		70	°C

Table 35
Capitance

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	CI	A0 - A13,CLK, CKE, /CS, /RAS, /CAS, /WE, DQM, UDQM, LDQM	2.5		4	pF
Data input/output capacitance	CI/O	DQ	4		6.5	pF

*Note: TA = 25 *C, f = 1 MHz*

Table 36
DC Characteristics 1

Parameter	Symbol	Test condition	Grade	Maximum.			Unit	Notes
				x4	x8	x16		
Operating current (Prefetch mode at one bank active)	ICC1P	tRC ≥ tRC(MIN.) Prefetch is executed one time during tRC.	-A70	90	90	90	mA	1
			-A80	85	85	85		
			-A10	80	80	80		
Operating current (Restore mode at one bank active)	ICC1R	tRC ≥ tRC(MIN.)	-A70	90	90	90	mA	1
			-A80	85	85	85		
			-A10	80	80	80		
Precharge standby current in power down mode	ICC2P	CKE ≤ VIL(MAX.), tCK = 15 ns		1	1	1	mA	
	ICC2PS	CKE ≤ VIL(MAX.), tCK = ∞		0.5	0.5	0.5		
Precharge standby current in non power down mode	ICC2N	CKE ≥ VIH(MIN.), tCK = 15 ns /CS≥VIH(MIN.), Input signals are changed one time during 30 ns.		25	25	25	mA	
	ICC2NS	CKE ≥ VIH(MIN.), tCK = ∞ Input signals are stable.		8	8	8		
Active standby current in power down mode	ICC3P	CKE ≤ VIL(MAX.), tCK = 15 ns		5	5	5	mA	
	ICC3PS	CKE ≤ VIL(MAX.), tCK = ∞		4	4	4		
Active standby current in non power down mode	ICC3N	CKE ≥ VIH(MIN.), tCK = 15 ns /CS ≥ VIH(MIN.) Input signals are changed one time during 30 ns.		25	25	25	mA	
	ICC3NS	CKE≥VIH(MIN.),tCK=∞ Input signals are stable.		10	10	10		
Operating current (Burst mode)	ICC4	tCK ≥ tCK(MIN.), IO = 0 mA, Background: precharge standby	-A70	60	70	100	mA	2
			-A80	55	60	90		
			-A10	45	50	75		
Auto refresh current	ICC5	tRC ≥ tRC(MIN.)	-A70	145	145	145	mA	3
			-A80	135	135	135		
			-A10	115	115	115		
Self refresh current	ICC6	CKE ≤ 0.2 V	-A70 -A80 -A10	1	1	1	mA	
			-A70L -A80L -A10L	TBD	TBD	TBD		

Note: 1. ICC1 depends on cycle rates. In addition to this, ICC1 is measured on condition that addresses are changed only one time during tCK(MIN.).
2. ICC4 depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, ICC4 is measured on condition that addresses are changed only one time during tCK(MIN.).
3. ICC5 is measured on condition that addresses are changed only one time during tCK(MIN.).

Table 37
DC Characteristics 2

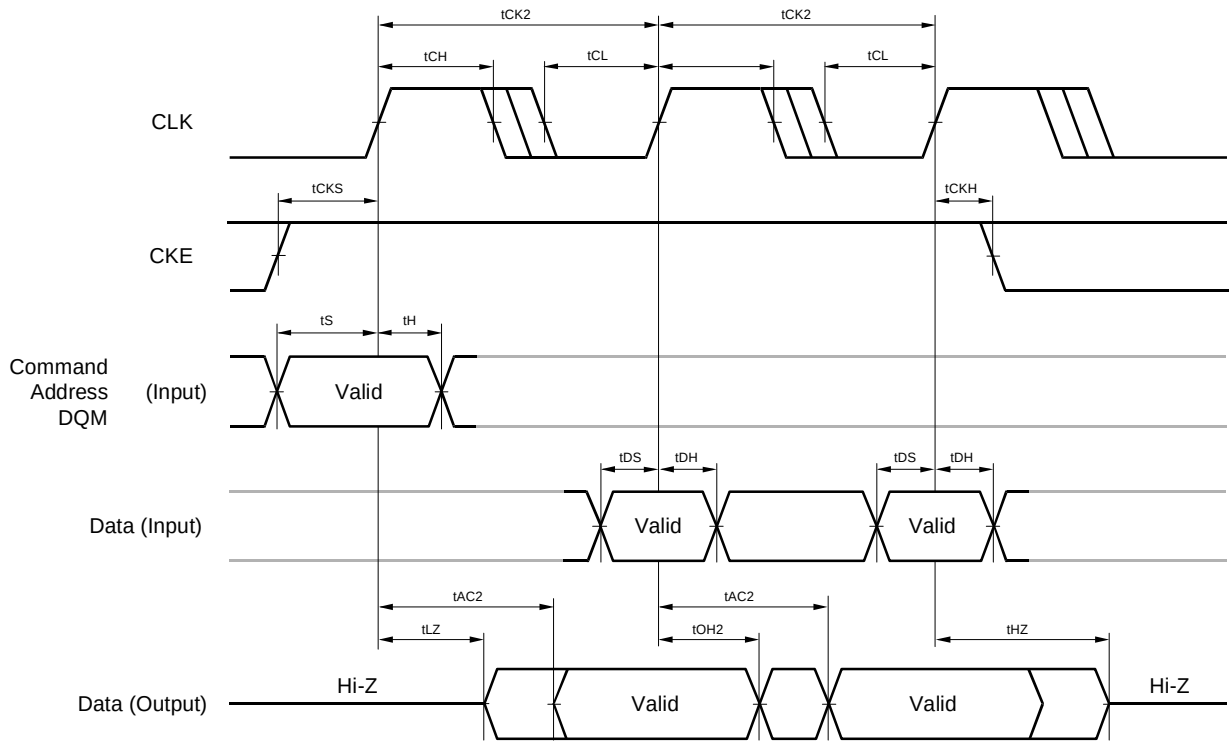
Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit	Note
Input leakage current	II(L)	VI = 0 to 3.6 V, All other pins not under test = 0 V	– 5.0	–	+ 5.0	?A	
Output leakage current	IO(L)	DOUT is disabled, VO = 0 to 3.6 V	– 5.0	–	+ 5.0	?A	
High level output voltage	VOH	IO = – 4 mA	2.4	–	–	V	
Low level output voltage	VOL	IO = + 4 mA	–	–	0.4	V	

3.2 AC Electrical Specifications

3.2.1 Test Conditions

- AC measurements assume tT = 1 ns.
- Reference level for measuring timing of input signals is 1.4 V. Transition times are measured between VIH and VIL.
- If tT is longer than 1 ns, reference level for measuring timing of input signals is VIH(MIN.) and VIL(MAX.).
- An access time is measured at 1.4 V.

Figure 42
Test Condition Timings



3.2.2 AC Characteristics

Table 38
AC Characteristics 1

Parameter	Symbol	- 7		- 7.5		- 10		- 15		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	ns	
Clock cycle time	t_{CK2}	7		7.5		10		15		ns	1
Access time from CLK	t_{AC2}		5.5		5.5		6		12	ns	
CLK high level width	t_{CH}	2.5		2.5		3		3		ns	
CLK low level width	t_{CL}	2.5		2.5		3		3		ns	1
Data-out hold time	t_{OH2}	2.5		2.5		3		3		ns	
Data-out low-impedance time	t_{LZ}	0		0		0		0		ns	
Data-out high-impedance time	t_{HZ}	2.5	5.5	2.5	5.5	3	6	3	6	ns	
Data-in setup time	t_{DS}	2		2		2		2		ns	
Data-in hold time	t_{DH}	1		1		1		1		ns	
Address, Command, DQM setup time	t_{S}	2		2		2		2		ns	
Address, Command, DQM setup time	t_{H}	1		1		1		1		ns	
CKE setup time	t_{CKS}	2		2		2		2		ns	
CKE hold time	t_{CKH}	1		1		1		1		ns	
CKE setup time @ power down exit	t_{CKSP}	2		2		2		2		ns	
Transition time	t_{T}	1	30	1	30	1	30	1	30	ns	
Refresh time	t_{REF}		64		64		64		64	ms	
Mode register set cycle time	t_{RSC}	2		2		2		2		CLK	

Note: 1: Output Load

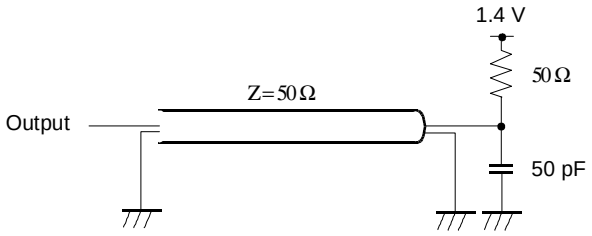


Table 39
AC Characteristics (Background to Background Operation)

Parameter	Symbol	- 7		- 7.5		- 10		- 15		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Same Bank Operation											
ACT to ACT / REF Command period	t_{RC}	70		75		80		90		ns	
REF to REF / ACT Command period	t_{RCF}	70		75		80		90		ns	
ACT to ACT / REF Command period (Prefetch to dummy and write to dummy channel with auto restore)	t_{RCPD}	119		120		160		165		ns	
ACT to PRE Command period	t_{RAS}	49	120k	52.5	120k	60	120k	60	120k	ns	
PRE to ACT / REF Command period	t_{RP}	20		20		20		30		ns	
ACT to PFC / PFCA / PFR / PFD / PPF / PPFA Command delay time	t_{APD}	15		15		20		30		ns	
ACT to PFC / PFCA / PFR / PFD / PPF / PPFA Command delay time (Prefetch Read Operation)	t_{APRD}	20		20		20		30		ns	
PFC to PRE Command delay time	t_{PPL}	21		22.5		30		30		ns	
PFCA / PFR to ACT / REF Command delay time	t_{PAL}	42		45		50		60		ns	
PPF to PRE Command delay time	t_{PPP}	42		45		60		75		ns	
PPFA to ACT / REFCommand delay time	t_{PPA}	63		67.5		80		90		ns	
RST / RSTA to ACT(R) Command delay time	t_{RAD}	7	28	7.5	30	10	40	10	60	ns	1, 2
Data-in to ACT / REF Command period (Write to dummy channel with auto restore)	t_{DAL}	77		82.5		110		120		ns	
Same, Other Bank Operation											
ACT(R) to PFC / PFCA / PFR / PFD / PPF / PPFA Command delay time	t_{RPD}	35		37.5		40		45		ns	1
PFC to PFC / PFCA Command delay time	t_{PPD}	21		22.5		30		30		ns	
PPF to PPF / PPFA Command delay time	t_{PPPD}	42		45		60		75		ns	
Other Bank Operation											
ACT to ACT / ACT(R) or ACT(R) to ACT Command delay time	t_{RRD}	14		15		20		30		ns	
ACT(R) to ACT(R) Command delay time	t_{RRDR}	28		30		40		45		ns	
PFC / PFCA to RST / RSTA Command delay time	t_{PRD}	21		22.5		30		30		ns	
PPF / PPFA to RST / RSTA Command delay time	t_{PPRD}	42		45		60		75		ns	

Note: 1. ACT(R) command is ACT command after RST command.
2. The another background operation and same channel foreground operation are illegal while t_{RAD} period.

Table 40
AC Characteristics (Foreground to Foreground Operation)

Parameter	Symbol	- 7		- 7.5		- 10		- 15		Units	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
READ / WRITE to READ / WRITE Command delay time	t_{CCD}	7		7.5		10		15		ns	

Table 41
AC characteristics (Background to Foreground operation; after same channel Prefetch/Restore)

Parameter	Symbol	- 7		- 7.5		- 10		- 15		Units	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
PFC / PFCA / PPF / PPFA to READ / WRITE and PFD to WRD / WRDA Command delay time	t_{PCD}	14		15		20		30		ns	
PPF / PPFA to READ / WRITE Command delay time	t_{PPCD}	35		37.5		50		75		ns	
ACT(R) to READ / WRITE Command delay time	t_{RCD}	28		30		40		45		ns	1

Note: 1: ACT(R) command is ACT command after RST command.

4 Timing Diagrams

Figure 43
Power on Sequence and Auto Refresh

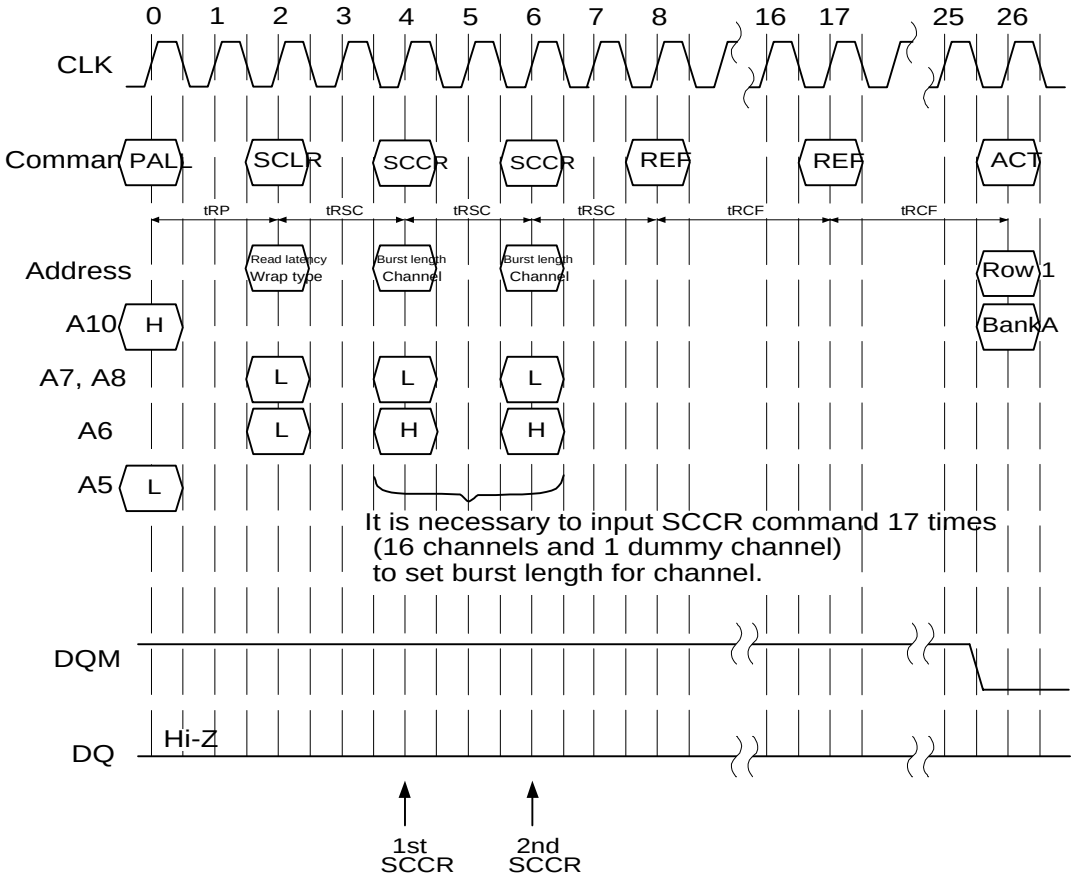


Figure 44
/CS Function (Only /CS signal needs to be issued at minimum rate)

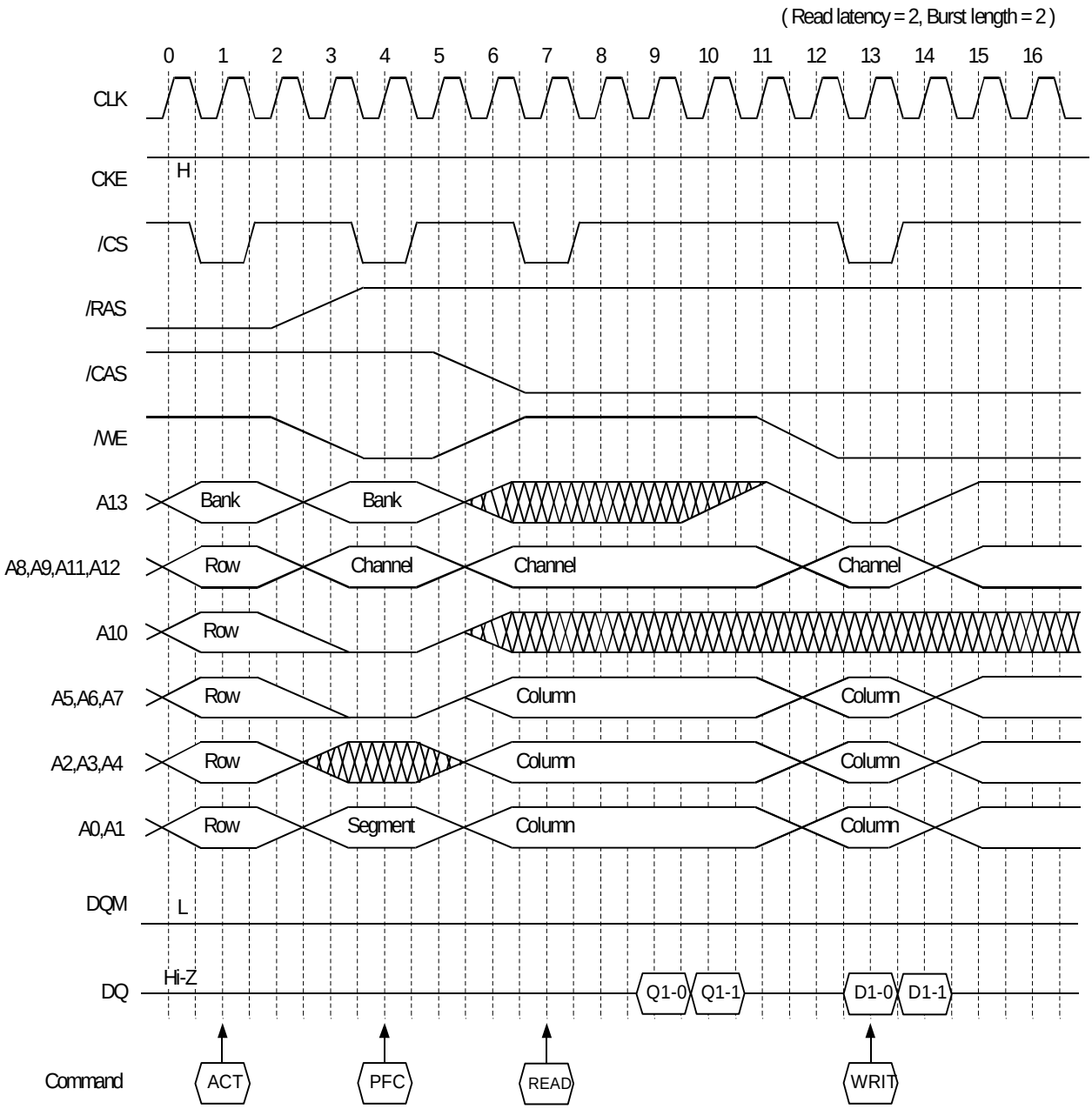


Figure 45
Clock Suspension during Burst Read (using CKE Function)

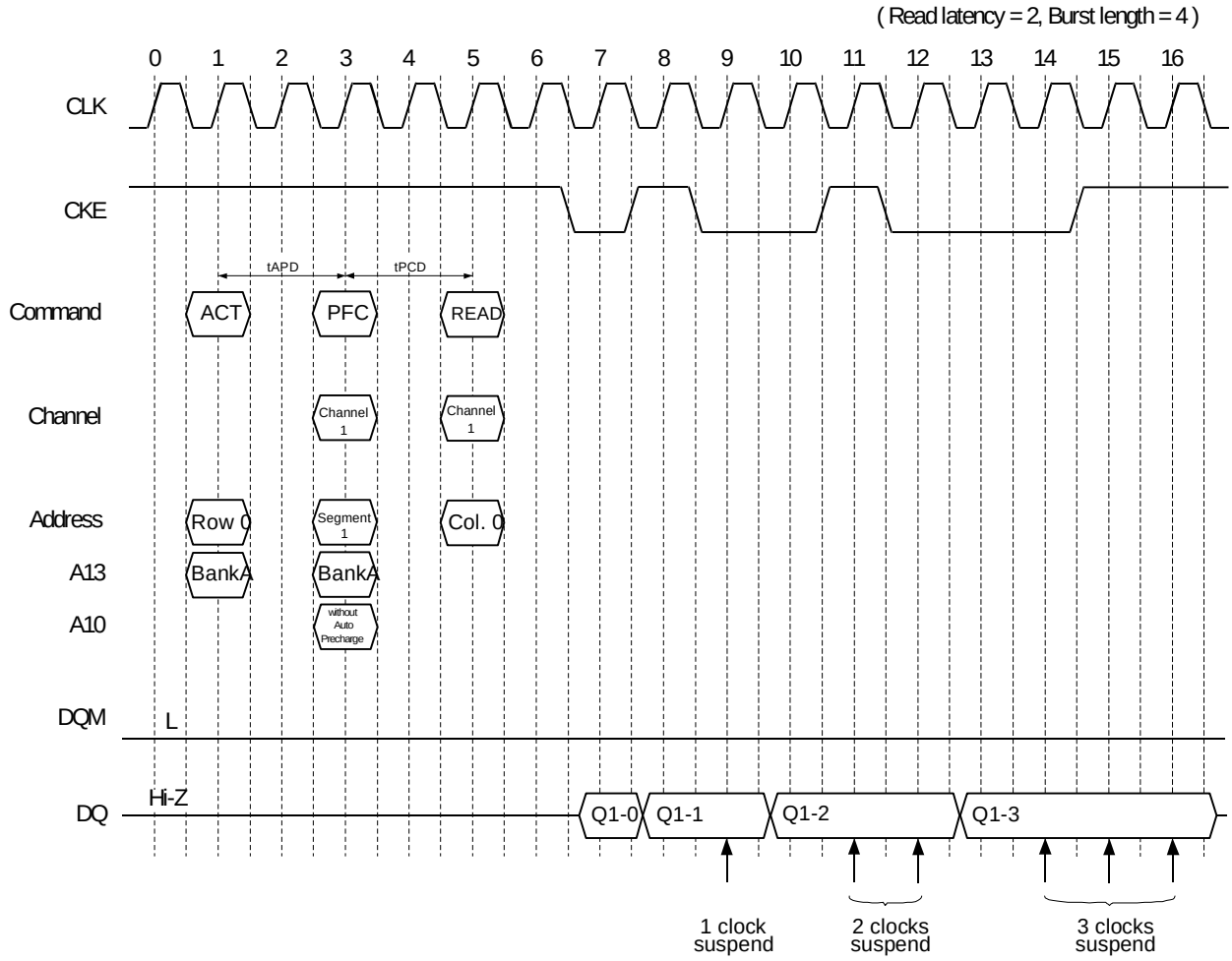


Figure 46
Clock Suspension during Burst Write (using CKE Function)

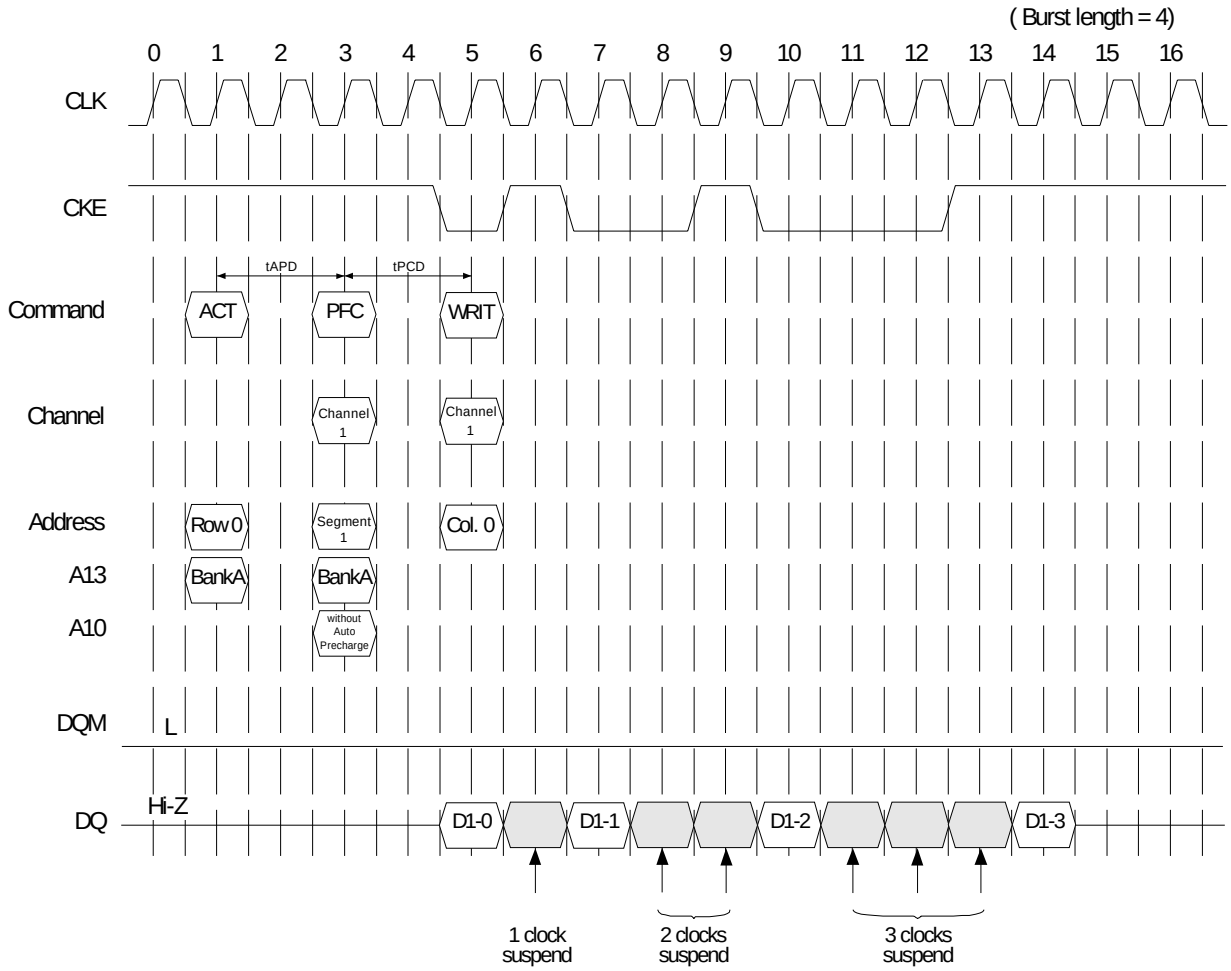


Figure 47
Power Down Mode

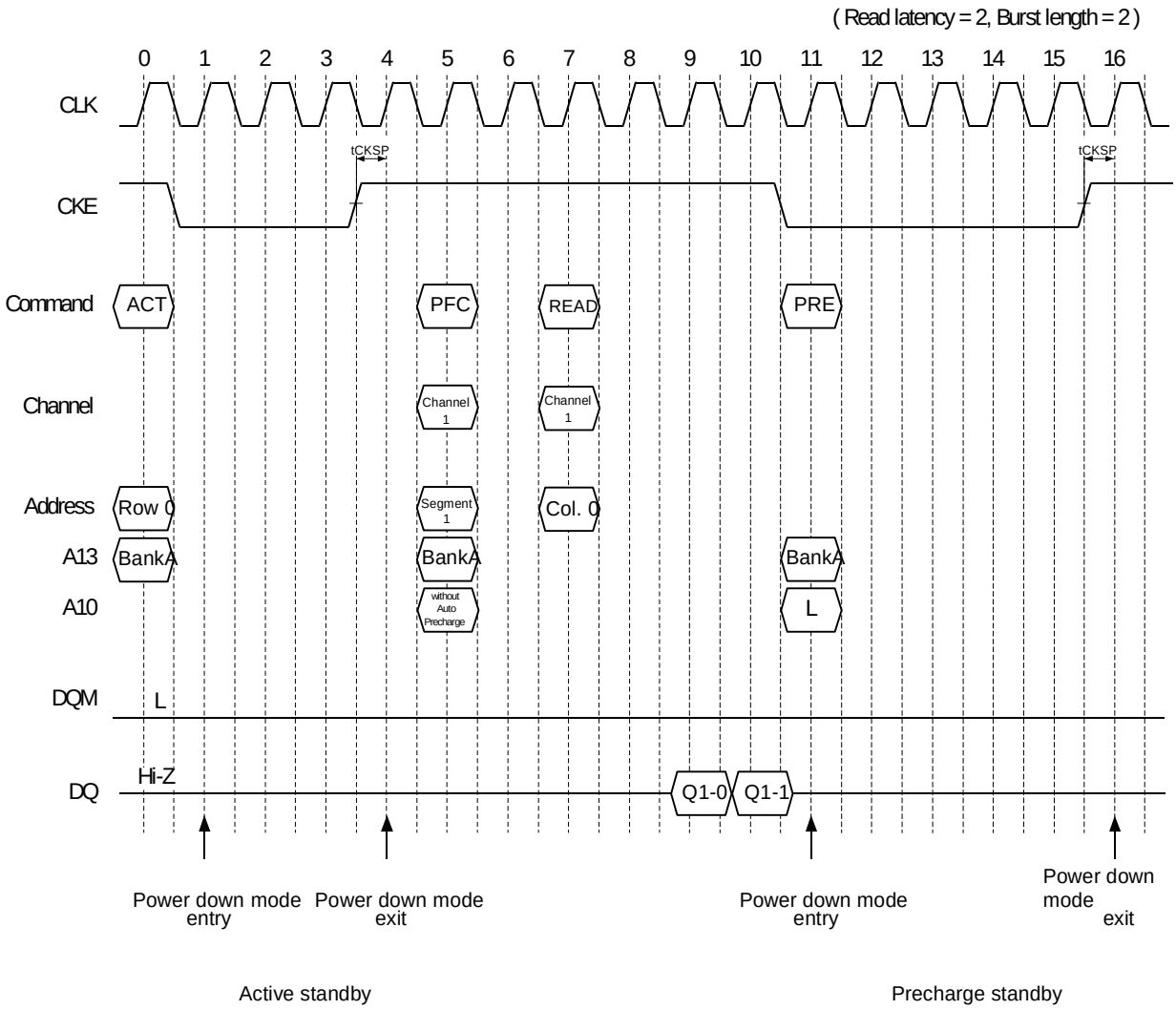


Figure 48
Set Register Operation

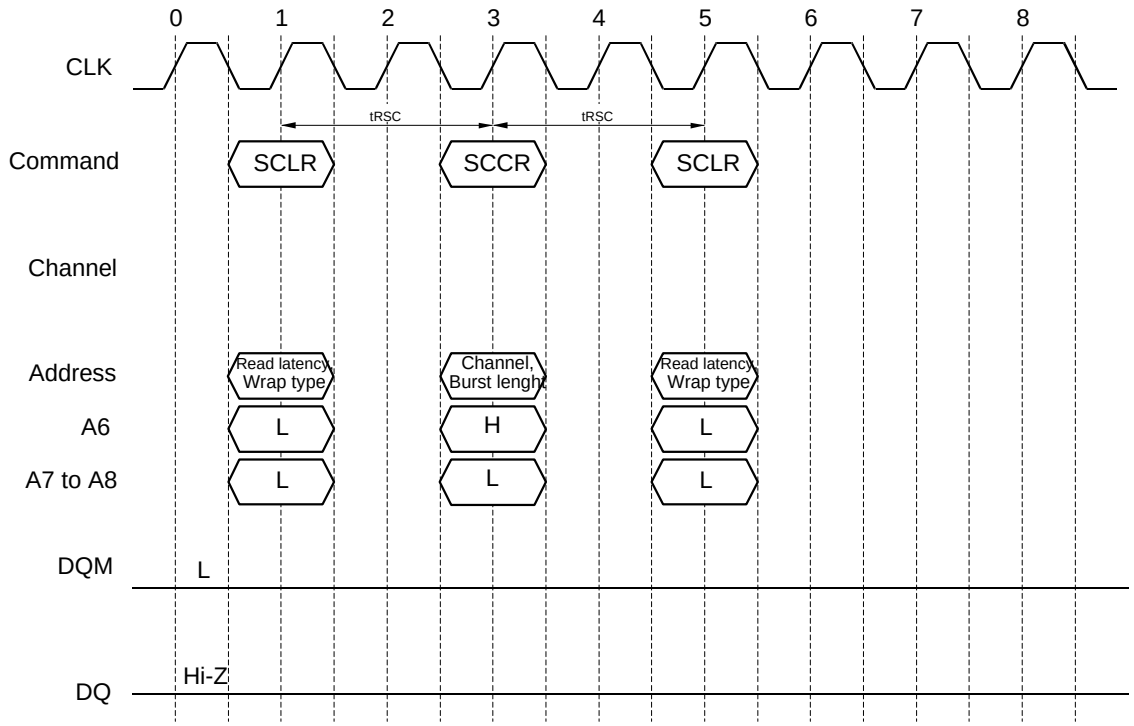


Figure 49
Read Operation

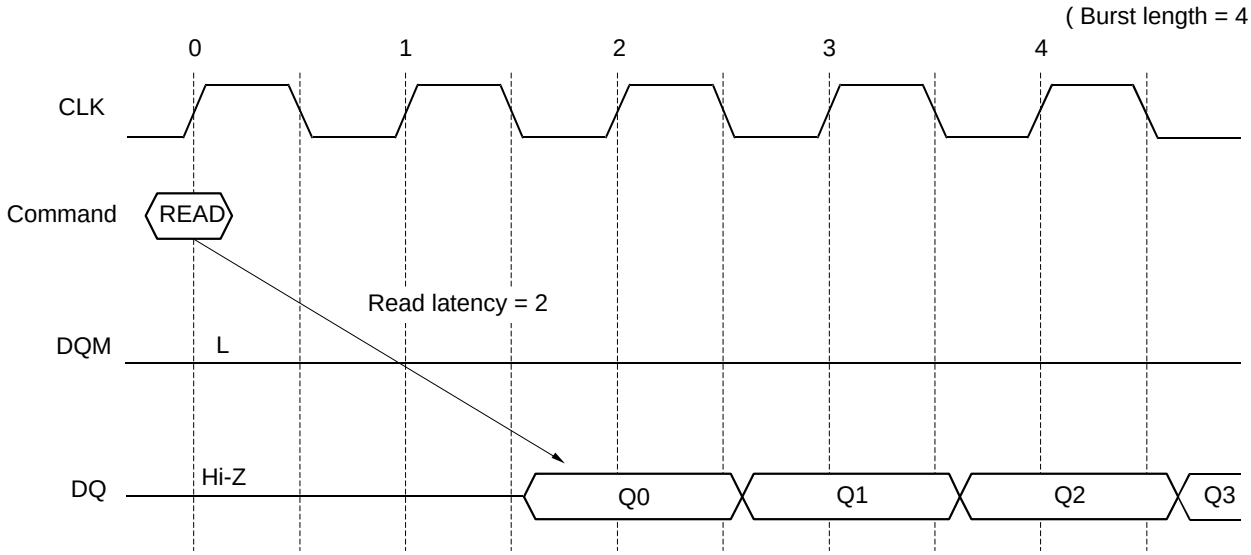


Figure 50
Write Operation

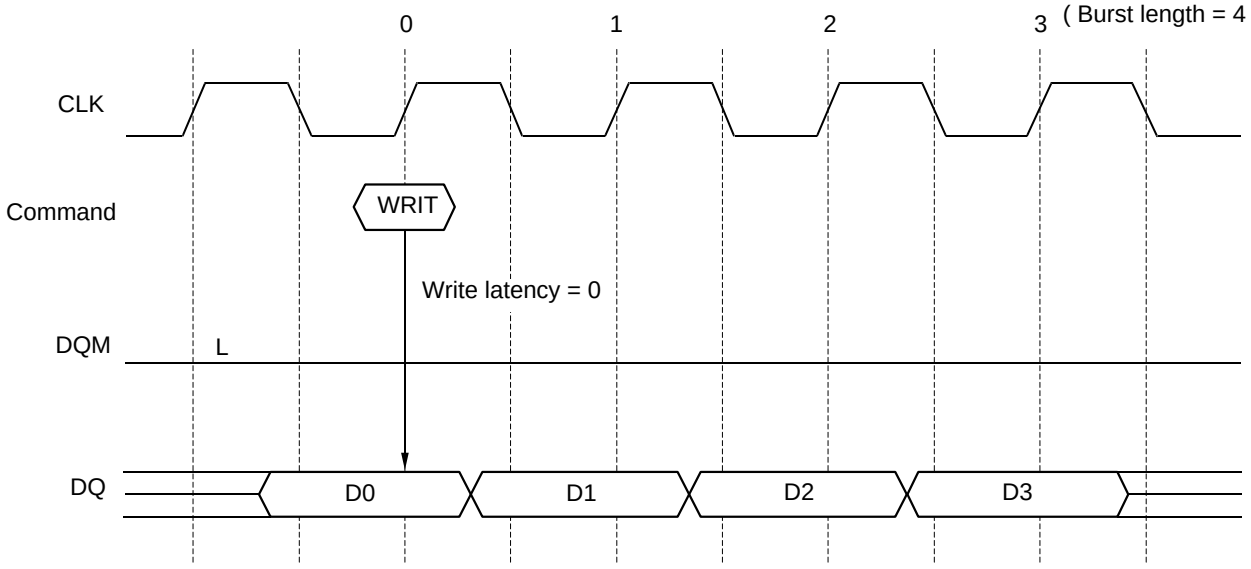


Figure 51
DQM Operation in READ

(Burst length = 4

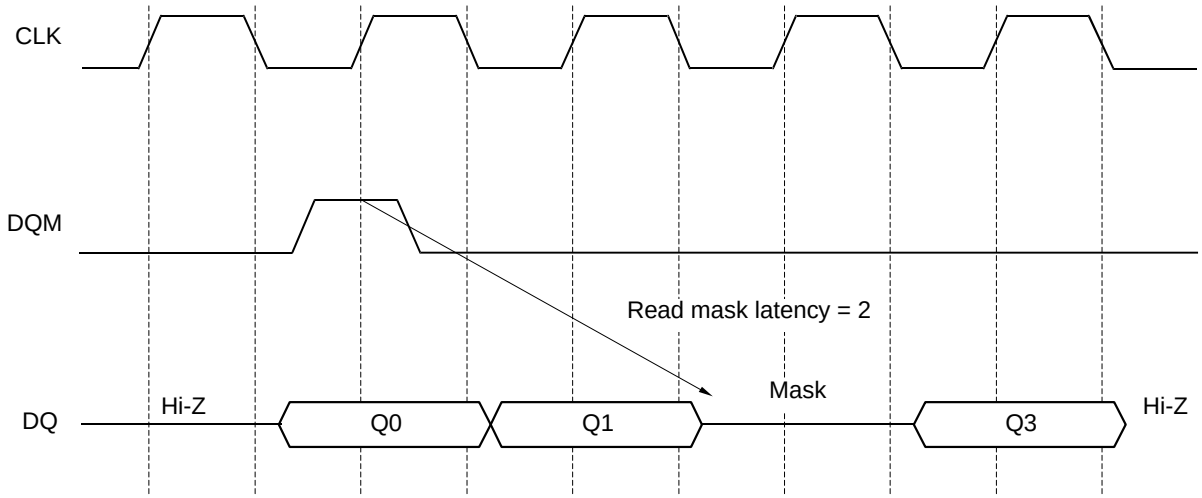


Figure 52
DQM Operation in WRITE

(Burst length = 4

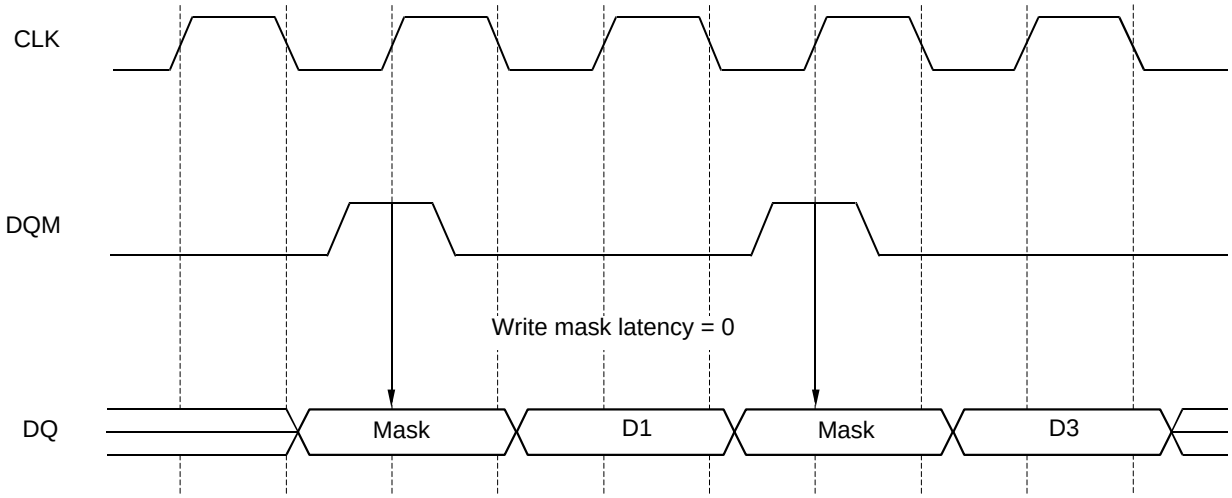


Figure 53
Read to Read Operation

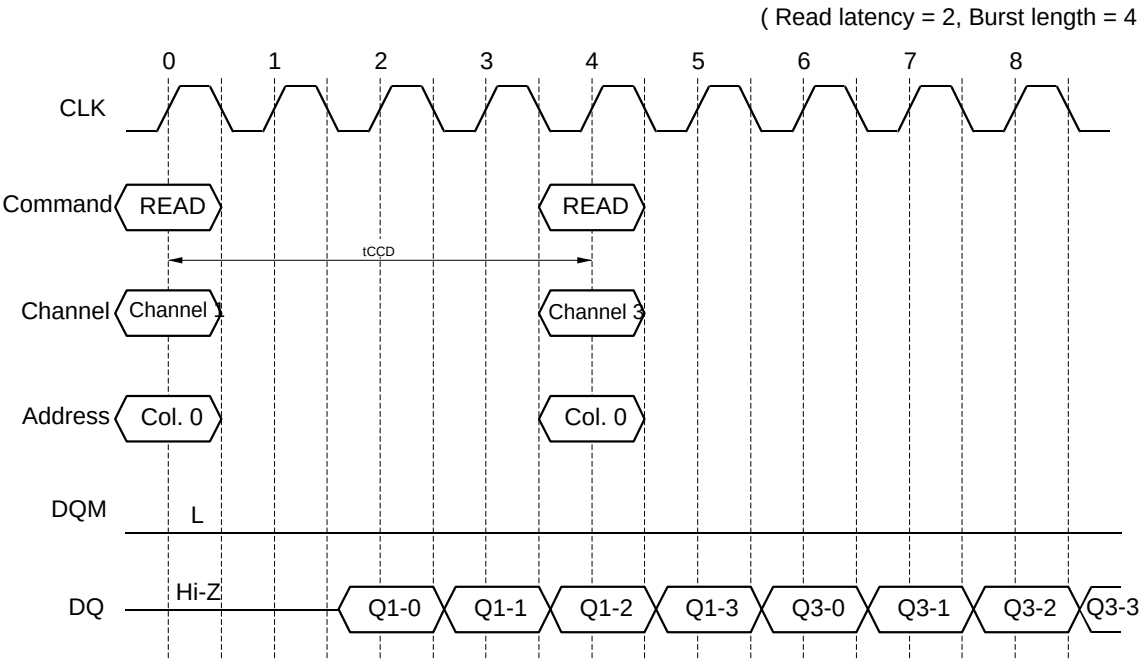


Figure 54
Write to Write Operation

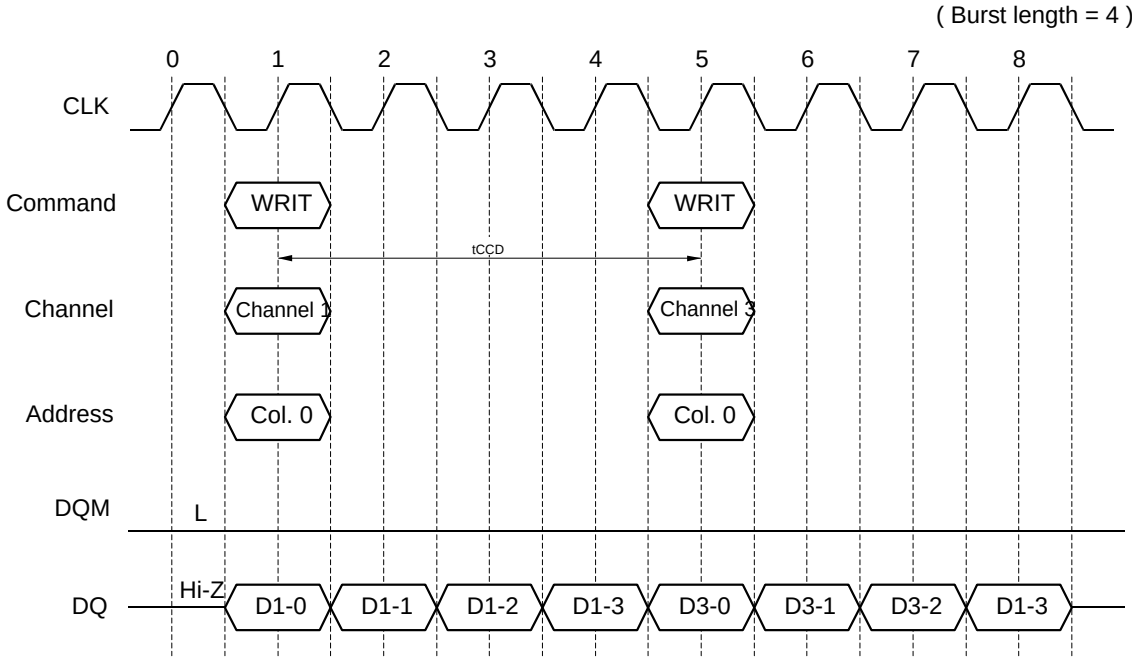


Figure 55
Read to Write Operation

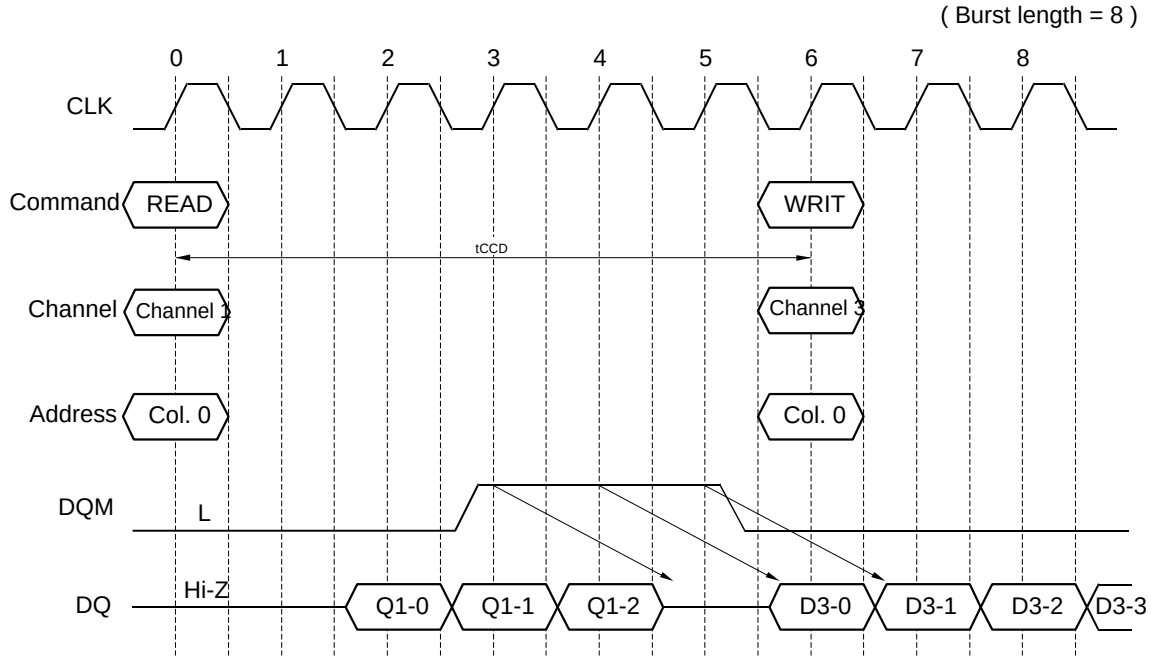


Figure 56
Write to Read Operation

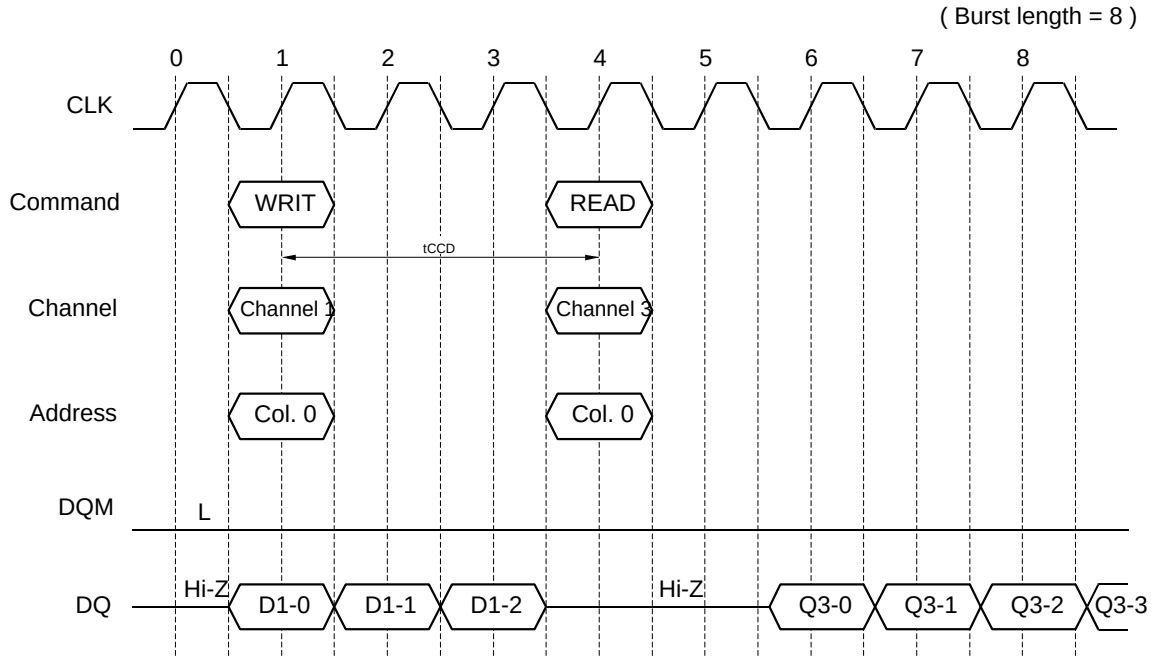


Figure 57
Prefetch to Read Operation without Auto Precharge (Same Channel Read)

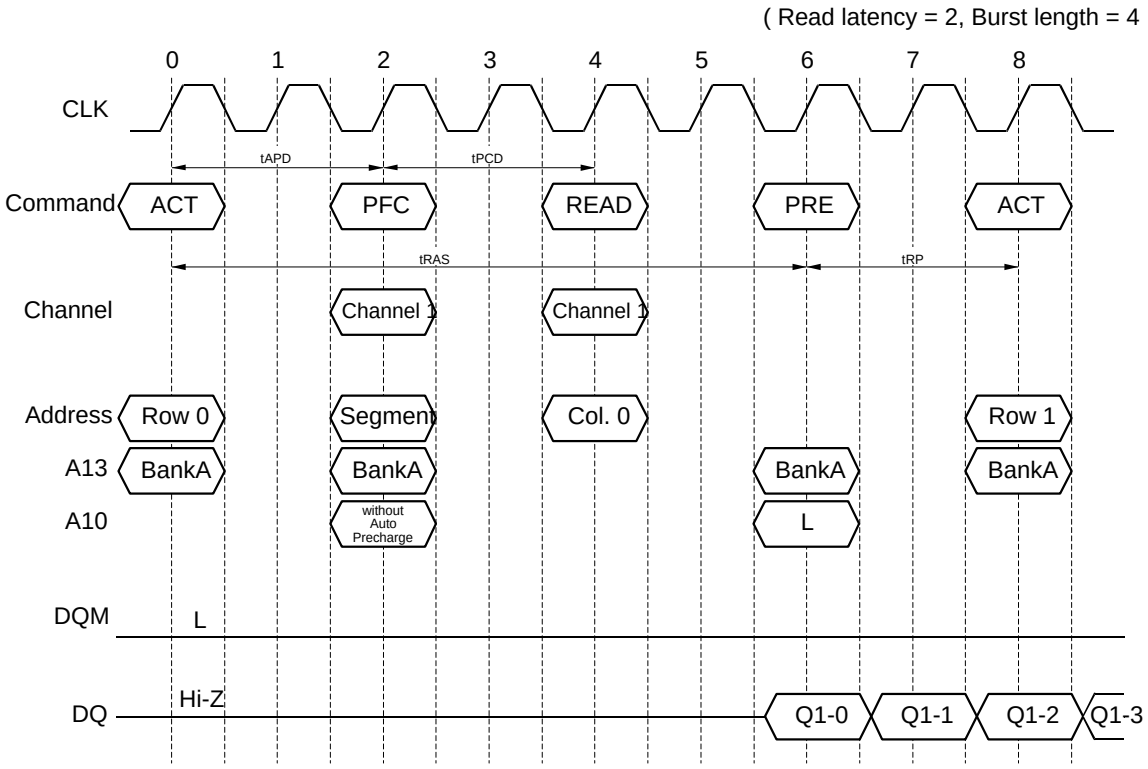


Figure 58
Prefetch to Read Operation without Auto Precharge (Other Channel Read)

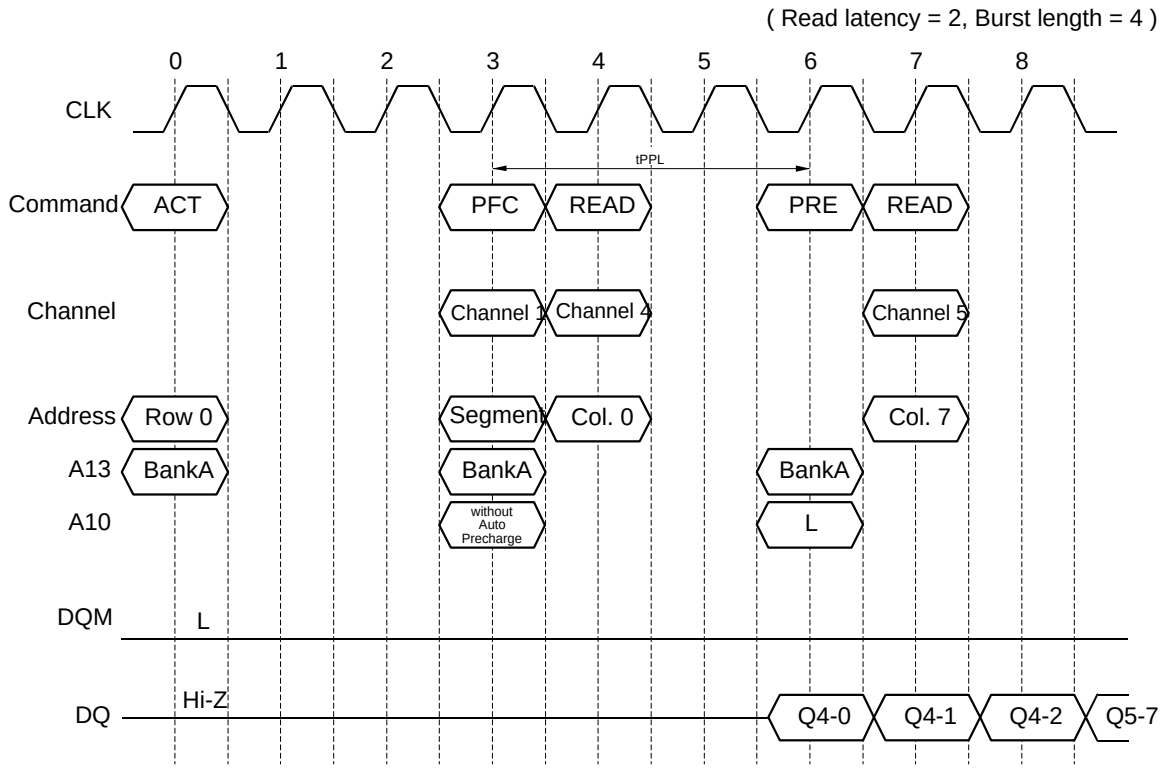


Figure 59
Prefetch to Write Operation without Auto Precharge (Same Channel Write)

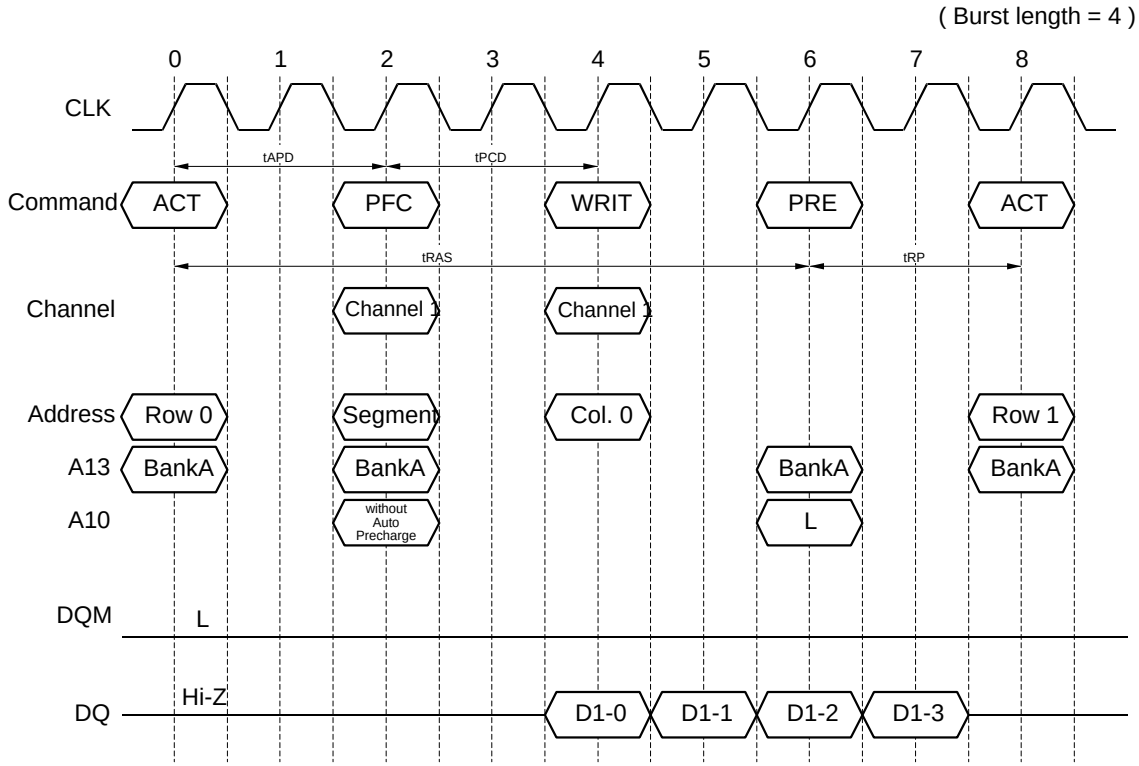


Figure 60
Prefetch to Write Operation without Auto Precharge (Other Channel Write)

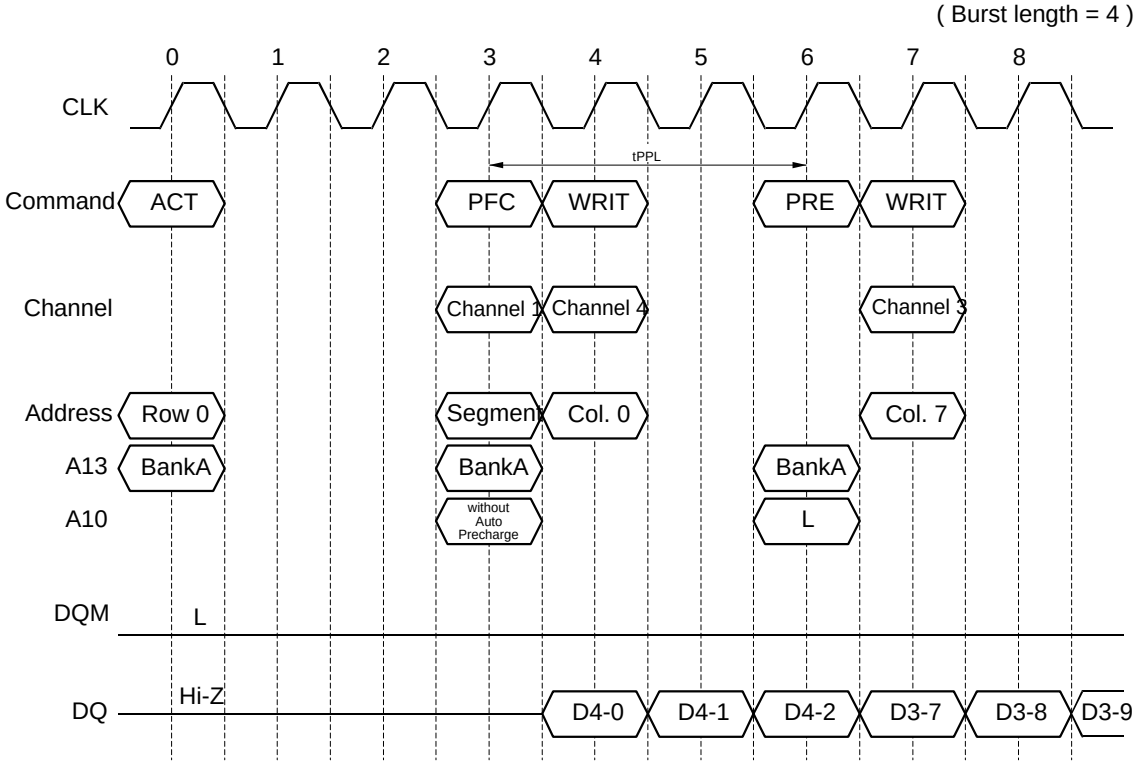


Figure 61
Read to Prefetch to Read Operation without Auto Precharge (Same Channel Prefetch)

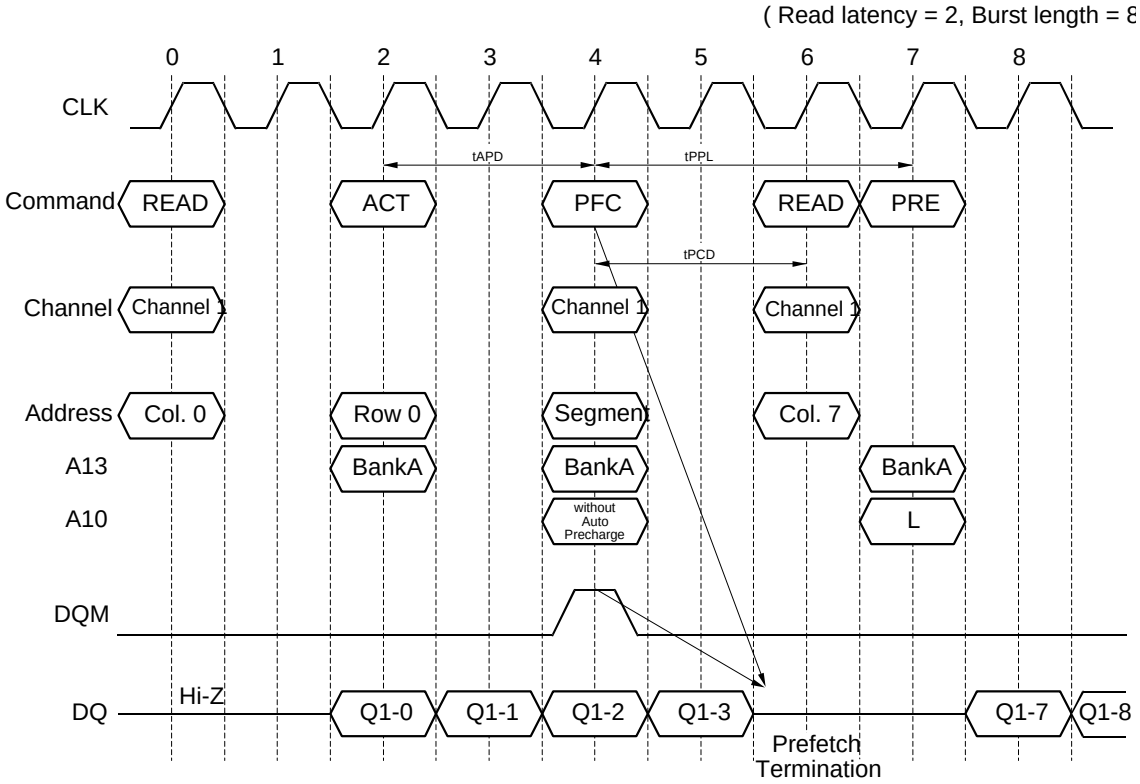


Figure 62
Read to Prefetch to Write Operation without Auto Precharge (Same Channel Prefetch)

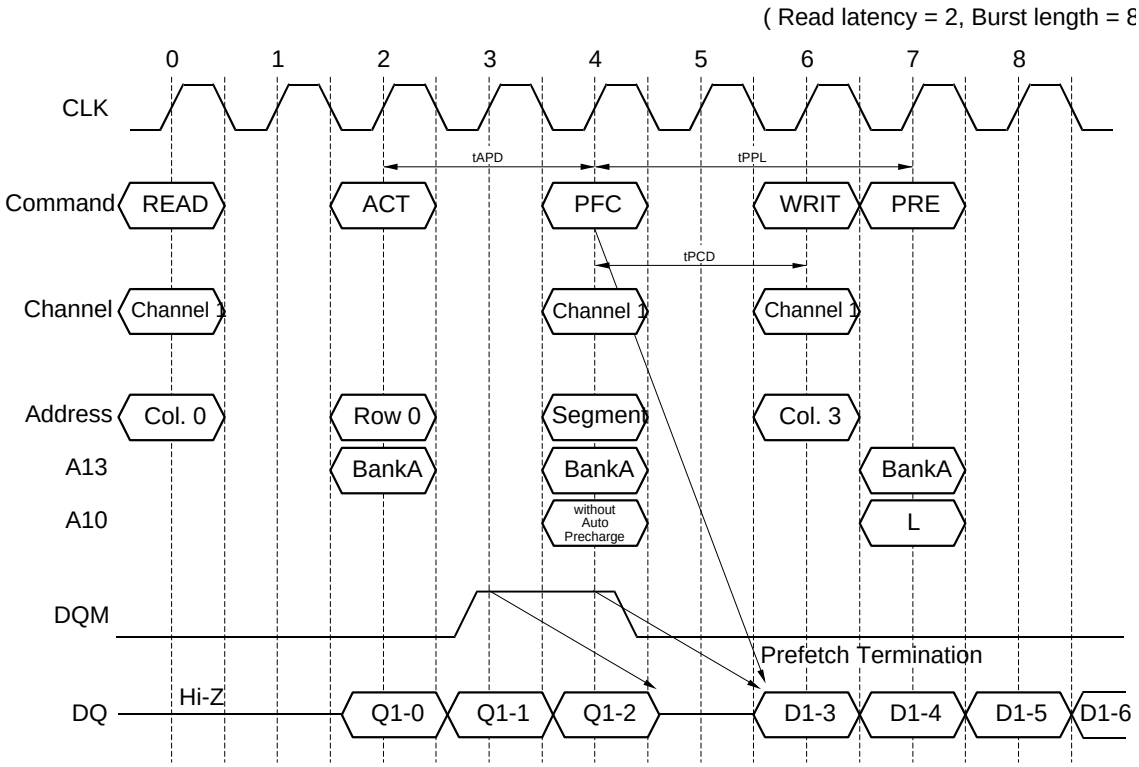


Figure 63
Write to Prefetch to Write Operation without Auto Precharge (Same Channel Prefetch)

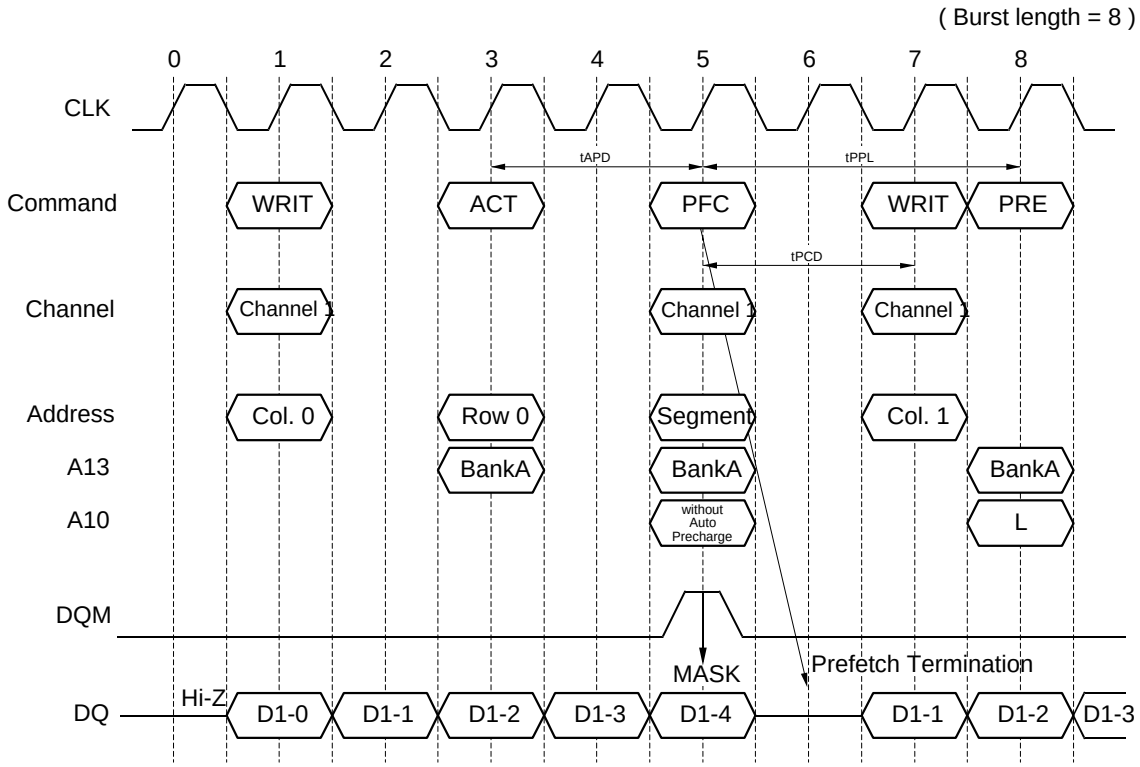


Figure 64
Write to Prefetch to Read Operation without Auto Precharge (Same Channel Prefetch)

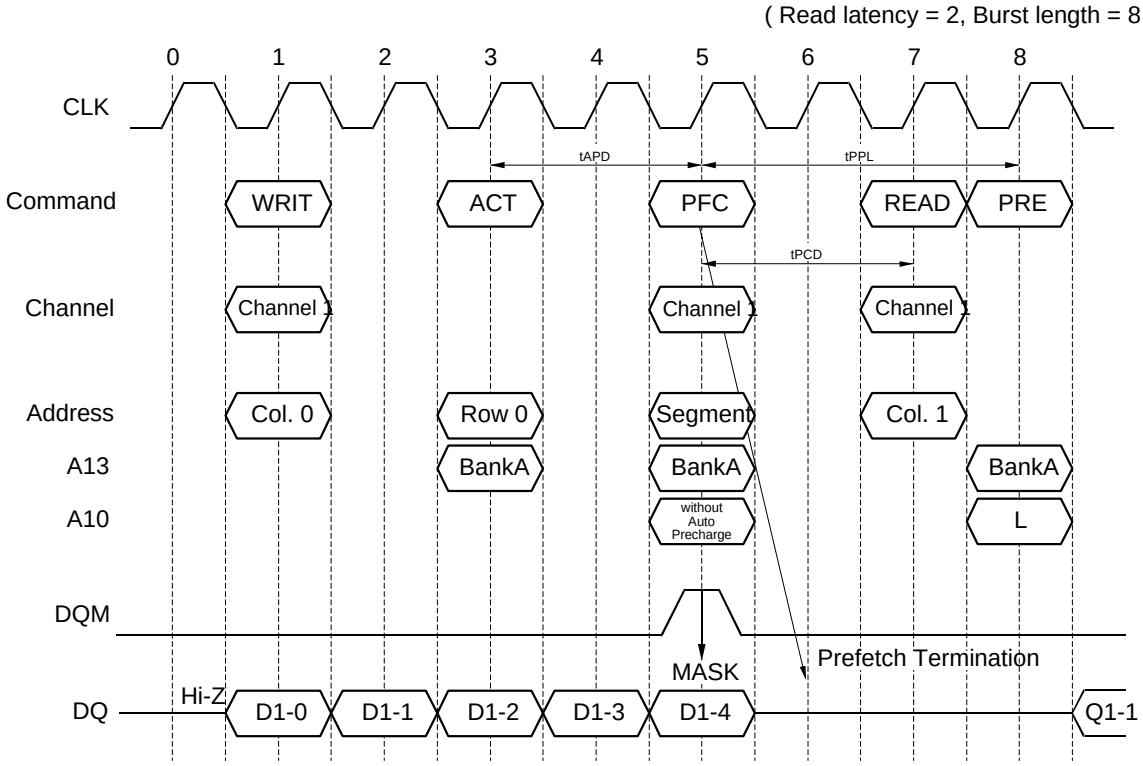
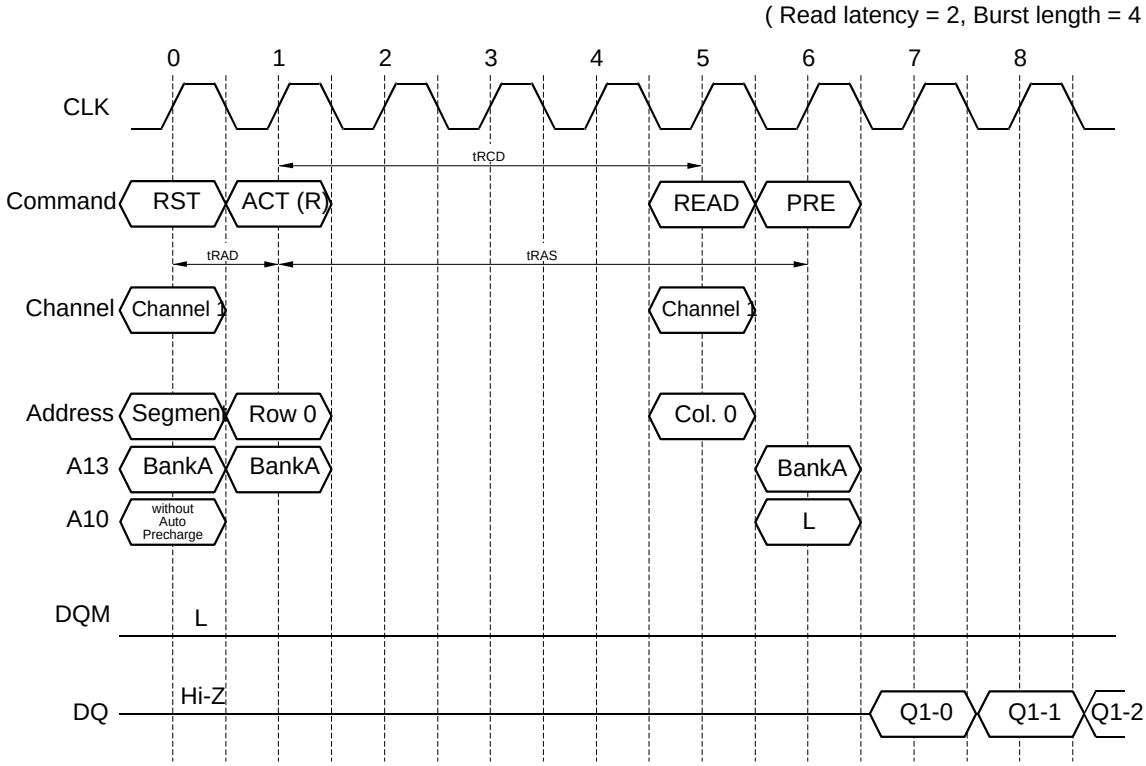
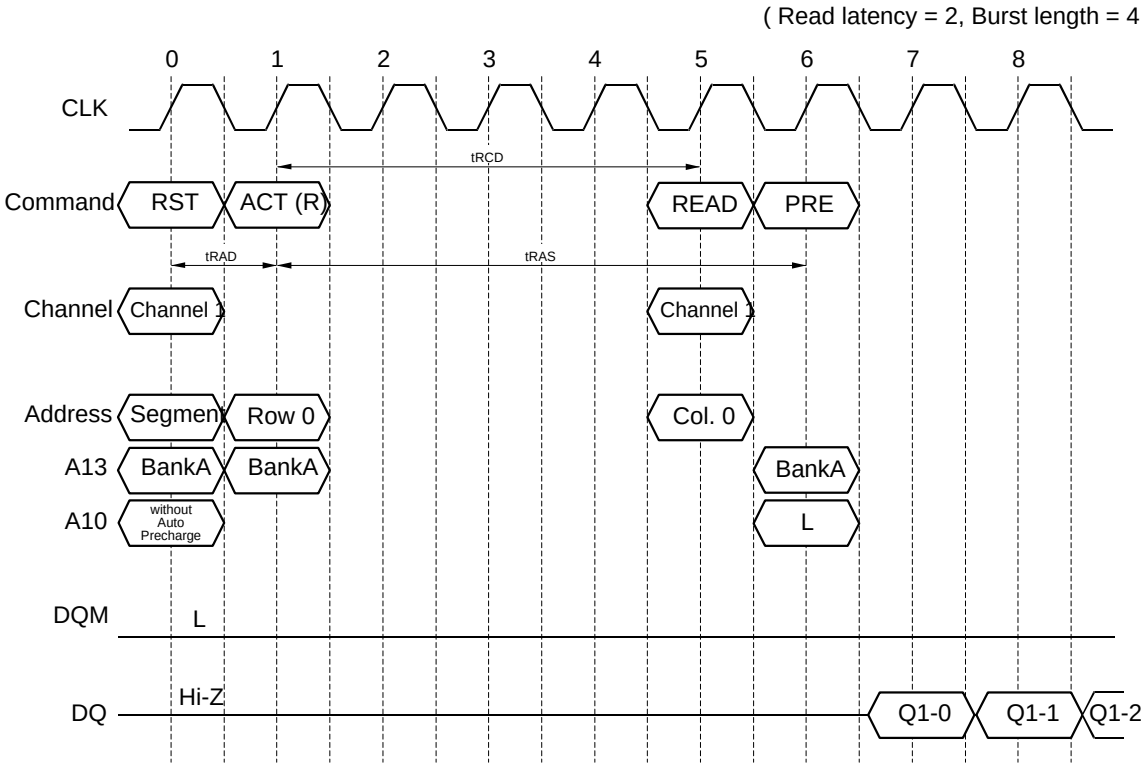


Figure 65
Restore to Read Operation without Auto Precharge (Same Channel Read)



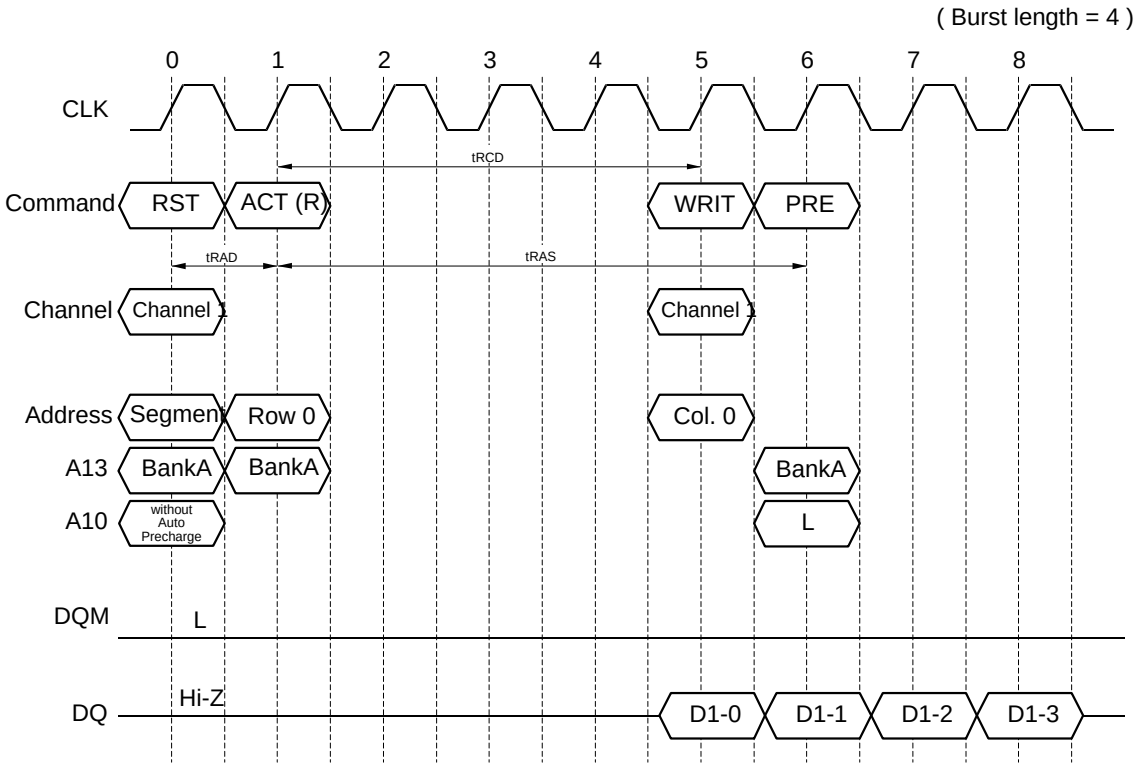
Remark ACT(R) command is ACT command after RST command.

Figure 66
Restore to Read Operation without Auto Precharge (Other Channel Read)



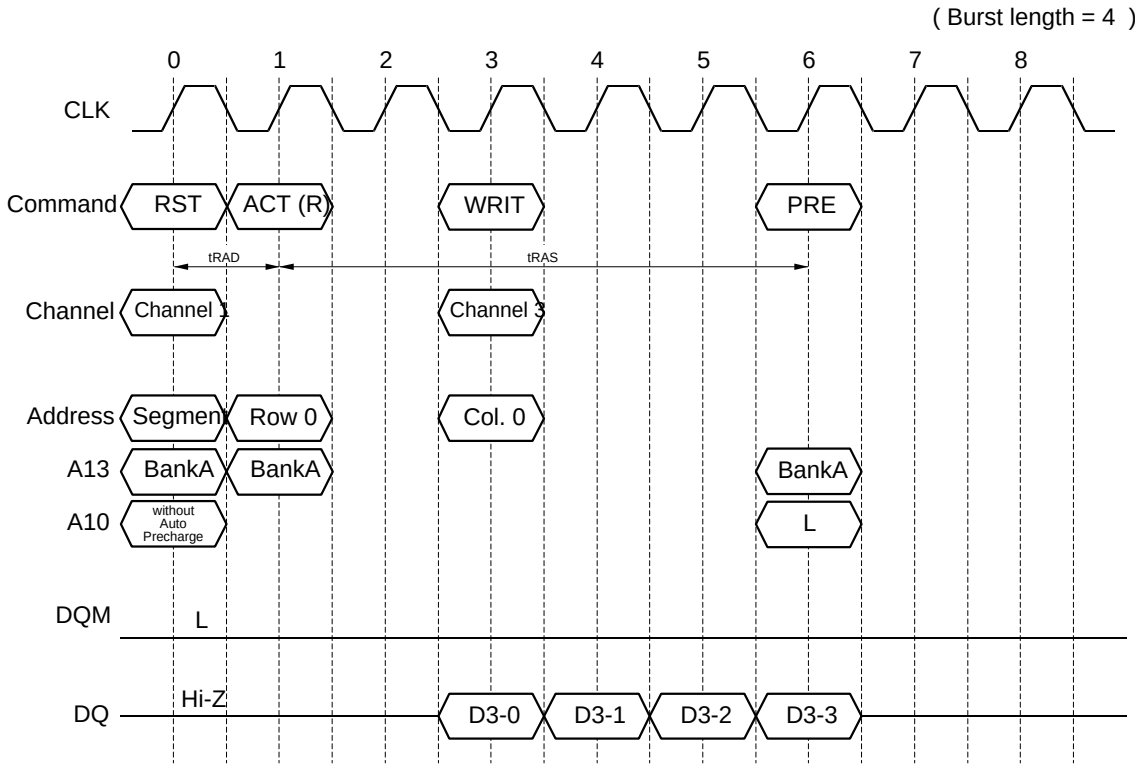
Remark ACT(R) command is ACT command after RST command.

Figure 67
Restore to Write Operation without Auto Precharge (Same Channel Write)



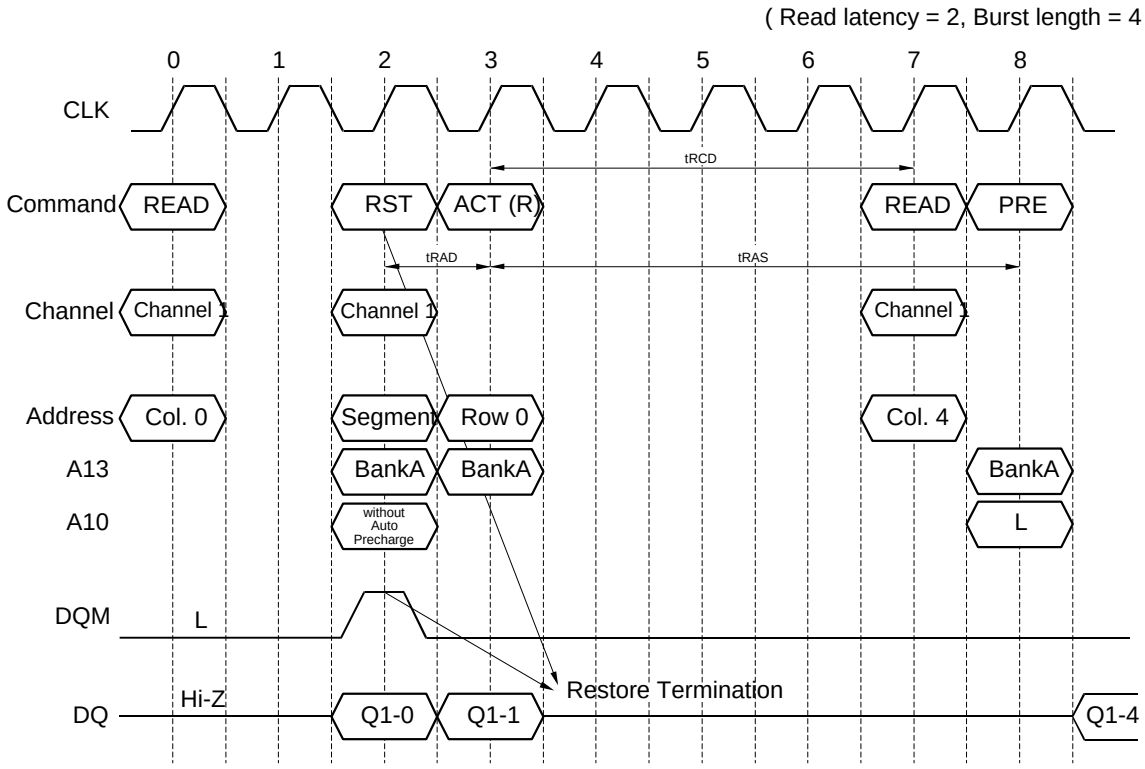
Remark ACT(R) command is ACT command after RST command.

Figure 68
Restore to Write Operation without Auto Precharge (Other Channel Write)



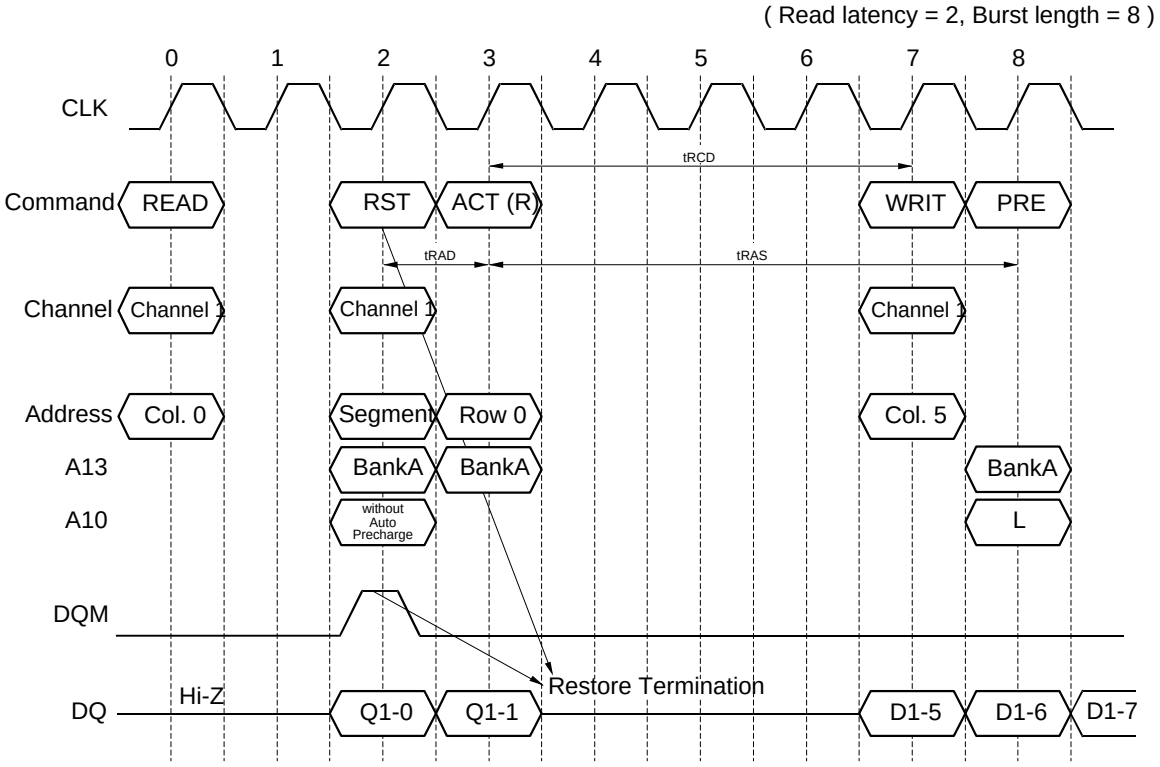
Remark ACT(R) command is ACT command after RST command.

Figure 69
Read to Restore to Read Operation without Auto Precharge (Same Channel Restore)



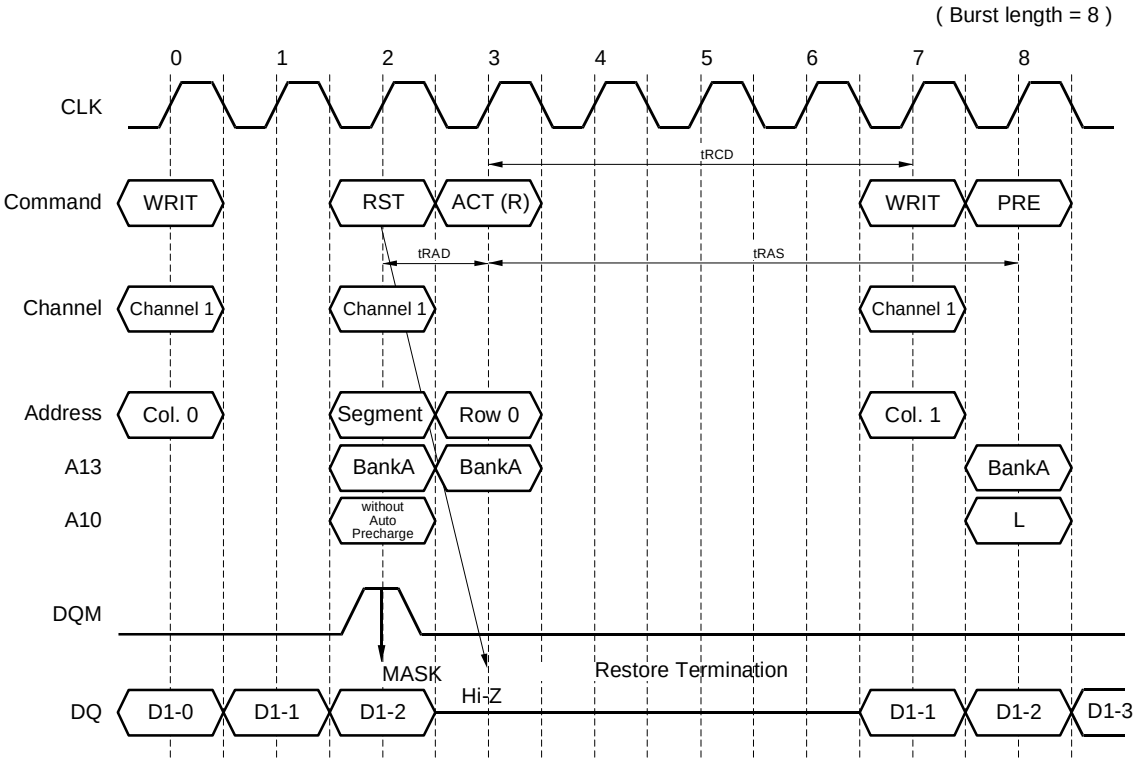
Remark ACT(R) command is ACT command after RST command.

Figure 70
Read to Restore to Write Operation without Auto Precharge (Same Channel Restore)



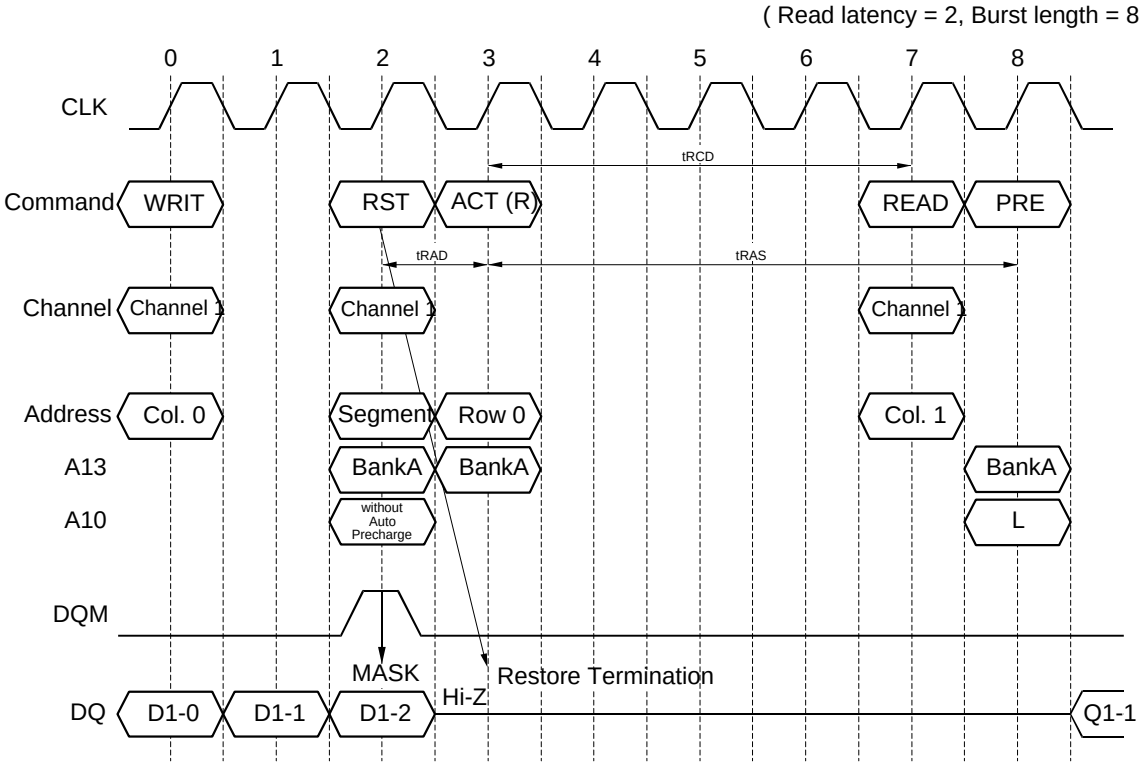
Remark ACT(R) command is ACT command after RST command.

Figure 71
Write to Restore to Write Operation without Auto Precharge (Same Channel Restore)



Remark ACT(R) command is ACT command after RST command.

Figure 72
Write to Restore to Read Operation without Auto Precharge (Same Channel Restore)



Remark ACT(R) command is ACT command after RST command.

Figure 73
Prefetch to Prefetch Operation without Auto Precharge

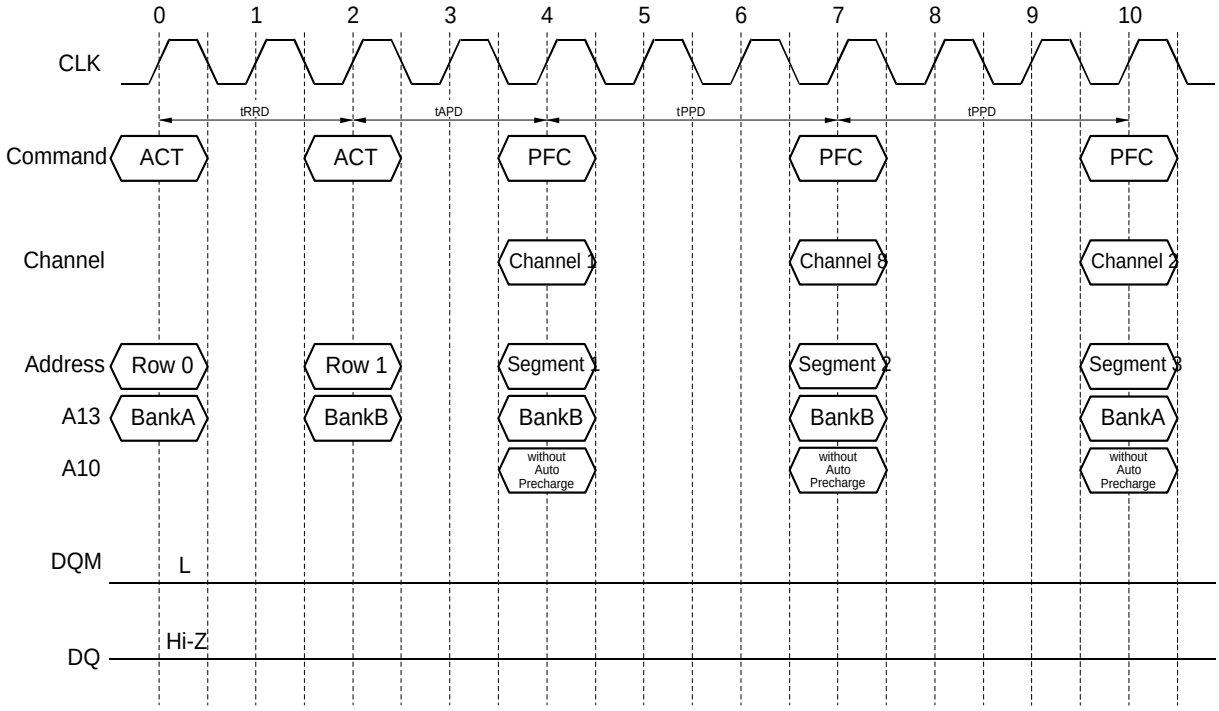
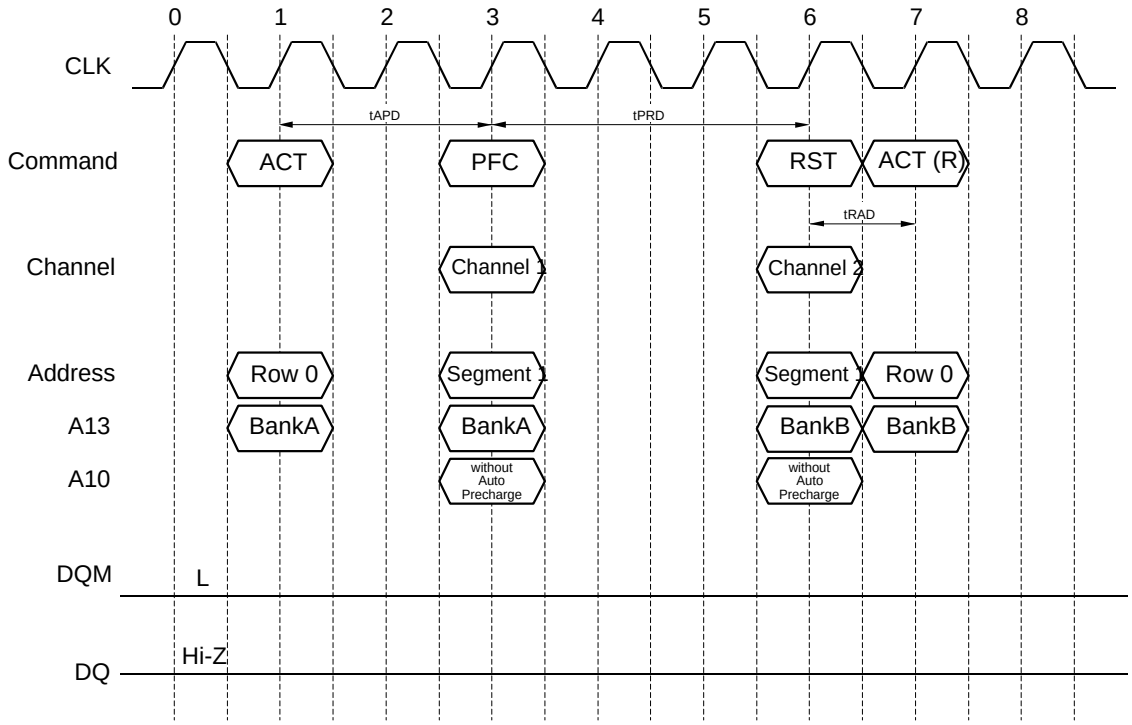


Figure 74
Prefetch to Restore Operation without Auto Precharge (Other Bank Restore)



Remark ACT(R) command is ACT command after RST command.

Figure 75
Prefetch Operation with Auto Precharge

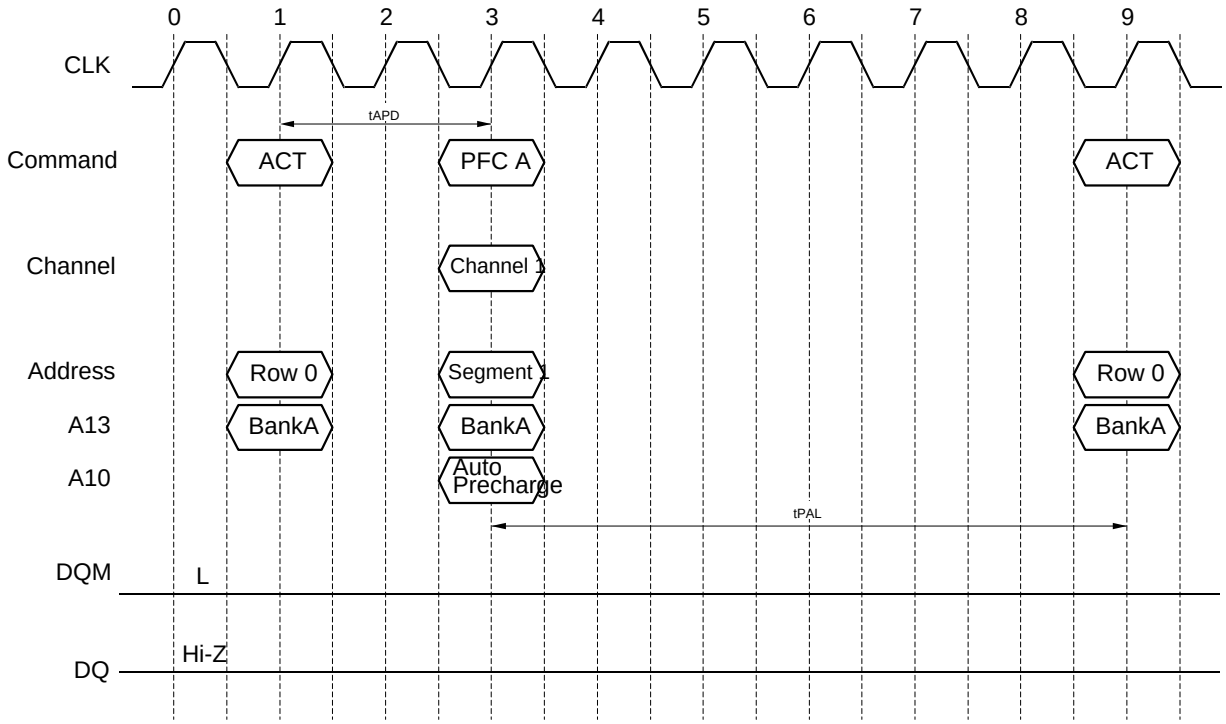
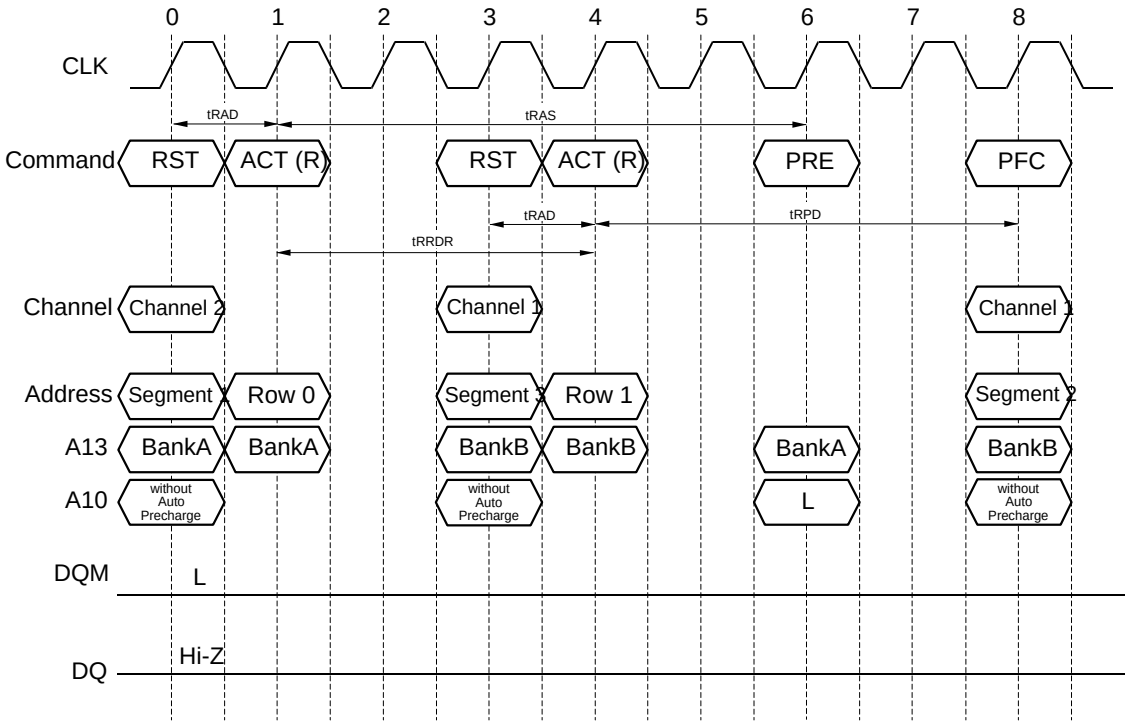
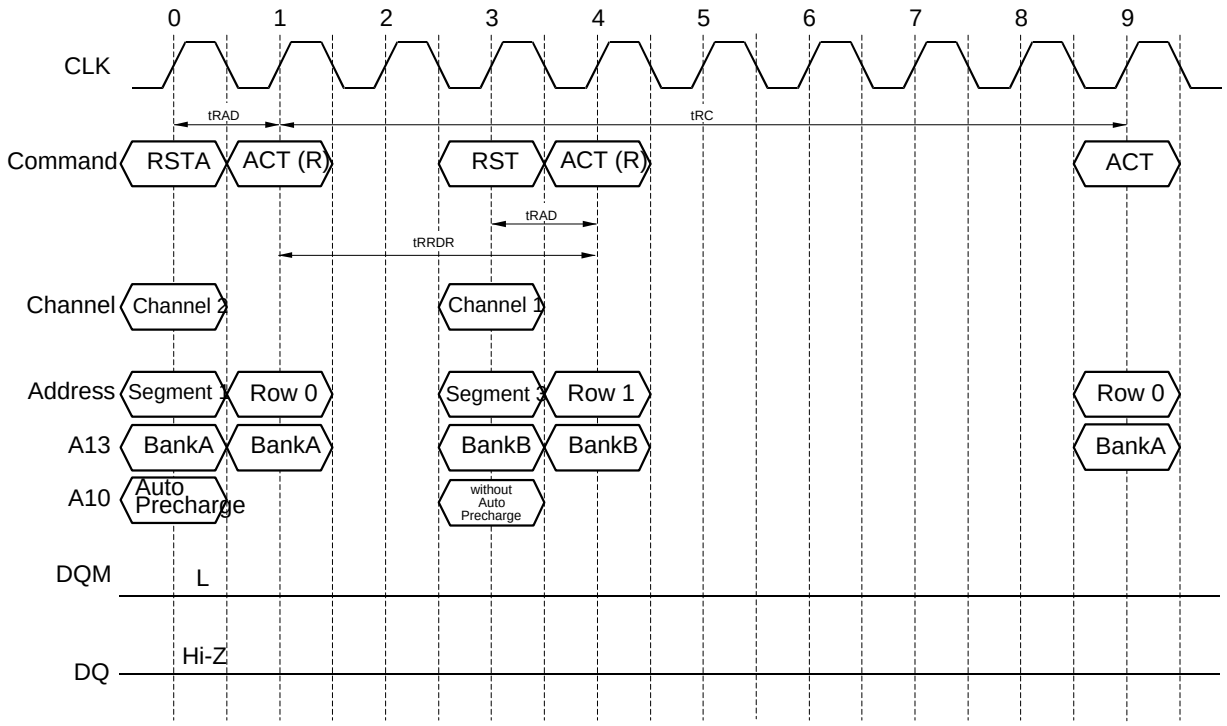


Figure 76
Restore to Prefetch Operation without Auto precharge



Remark ACT(R) command is ACT command after RST command.

Figure 77
Restore Operation with Auto Precharge



Remark ACT(R) command is ACT command after RST command.

Figure 78
Read to Prefetch Read with Auto Precharge Operation

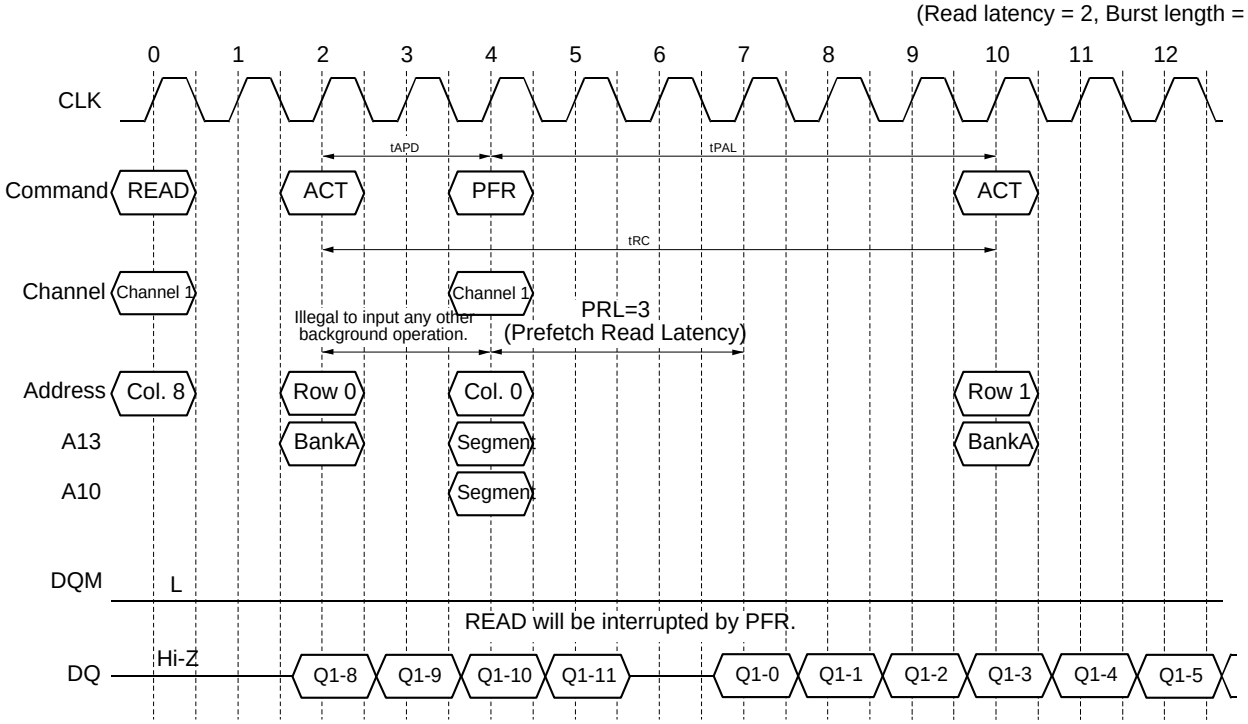


Figure 79
Write to Prefetch Read with Auto Precharge Operation

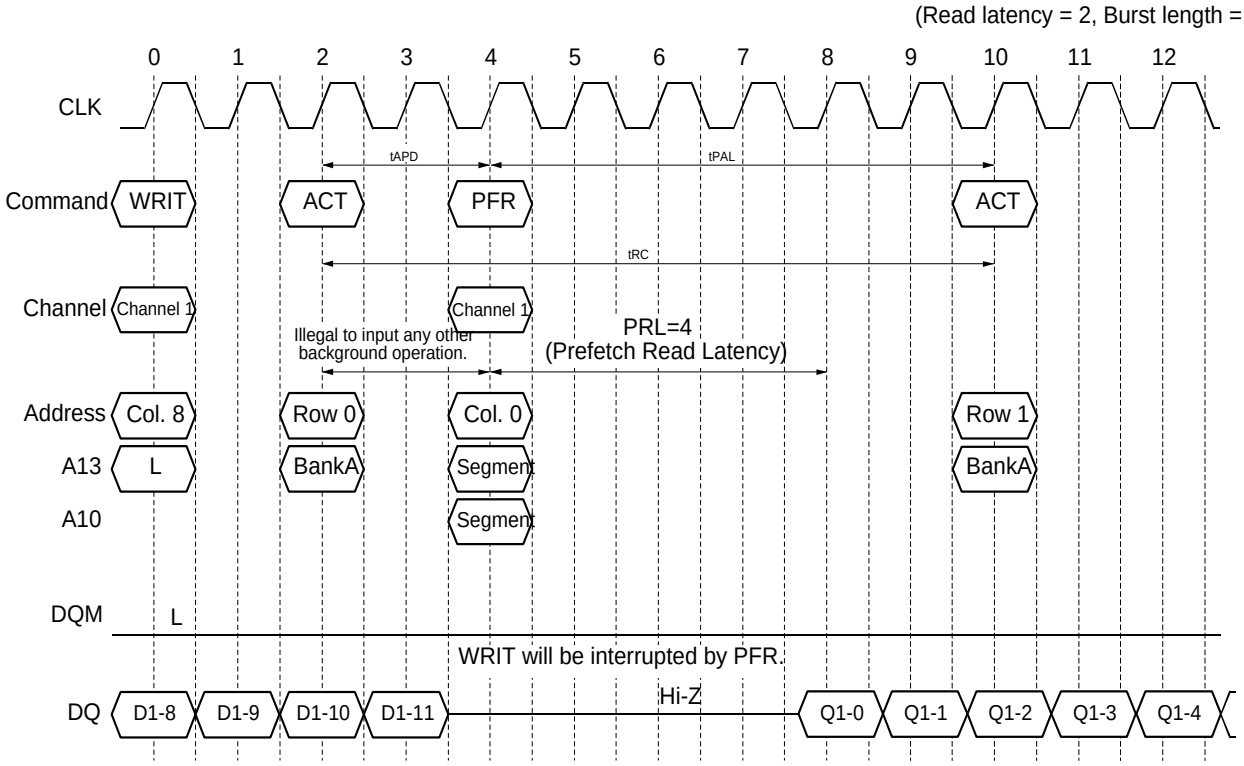


Figure 80
Prefetch to Dummy and Write to Dummy with Auto Restore Operation

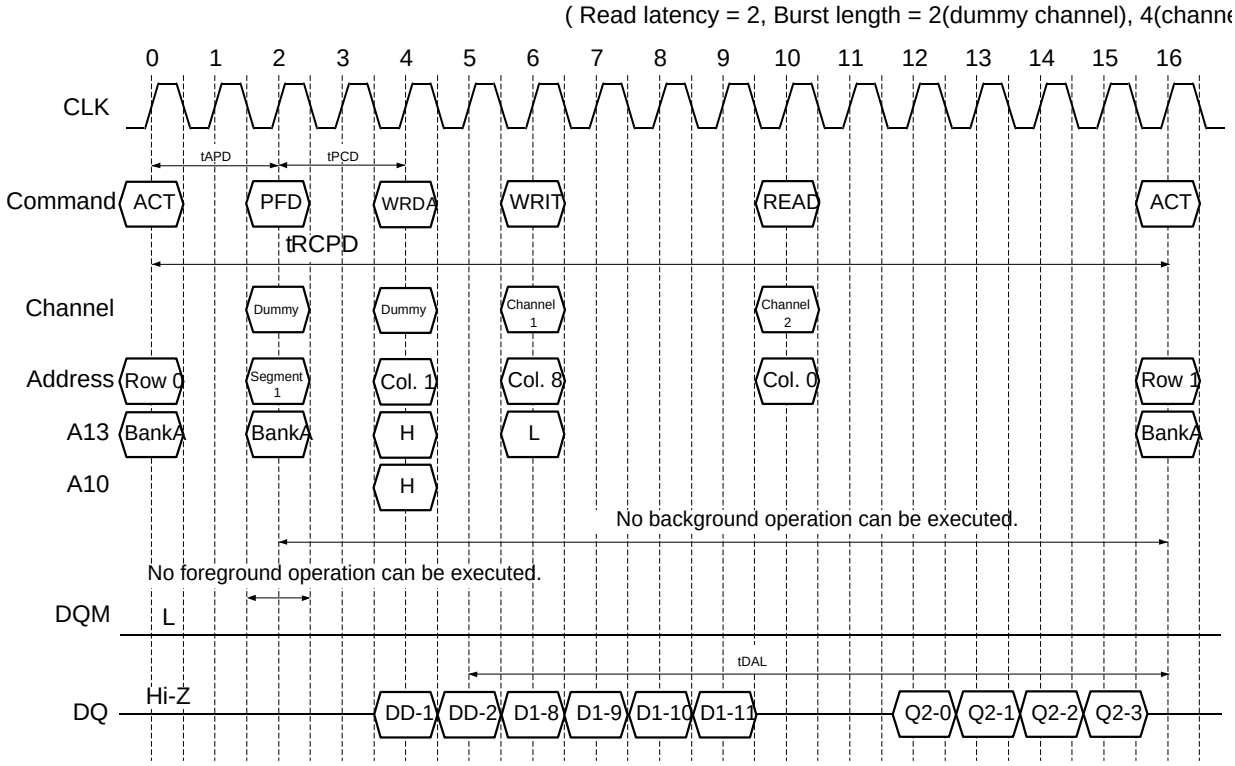


Figure 81
Prefetch to Dummy and Write to Dummy with Auto Restore Operation

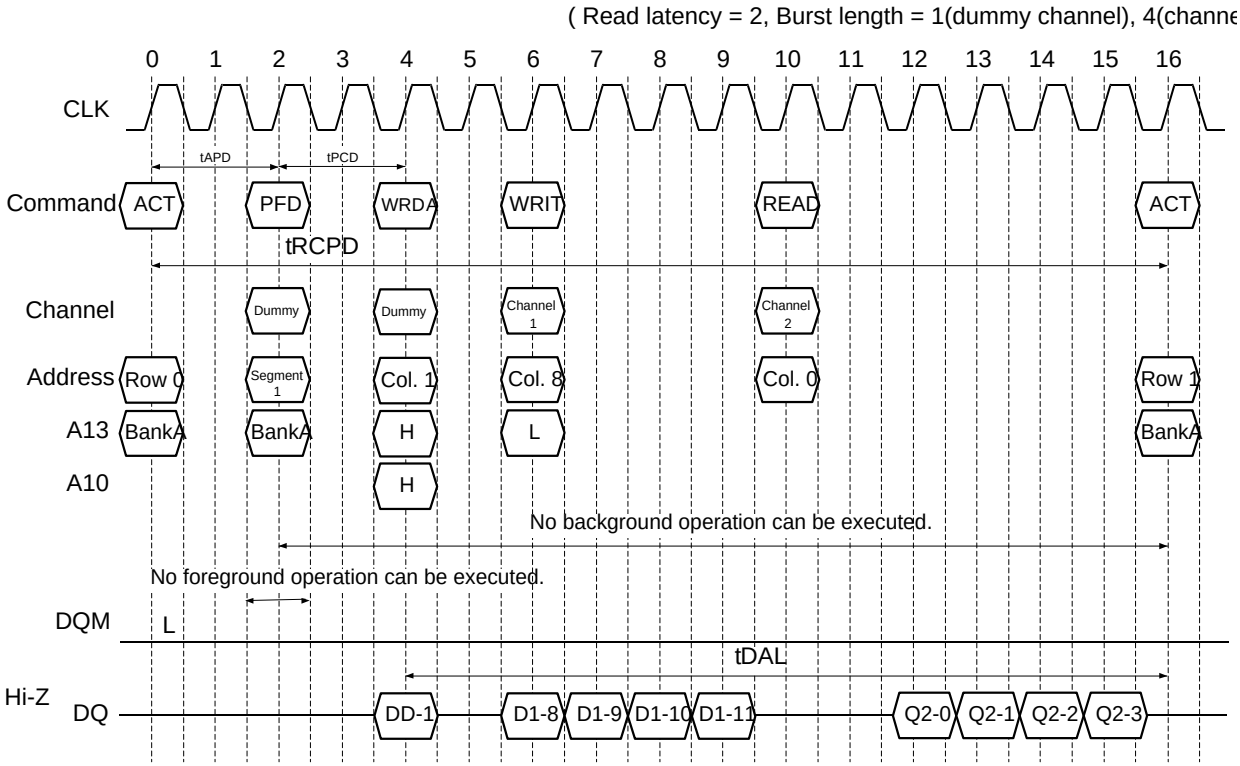


Figure 82
Prefetch to Dummy, Write to Dummy and Write to Dummy with Auto Restore Operation

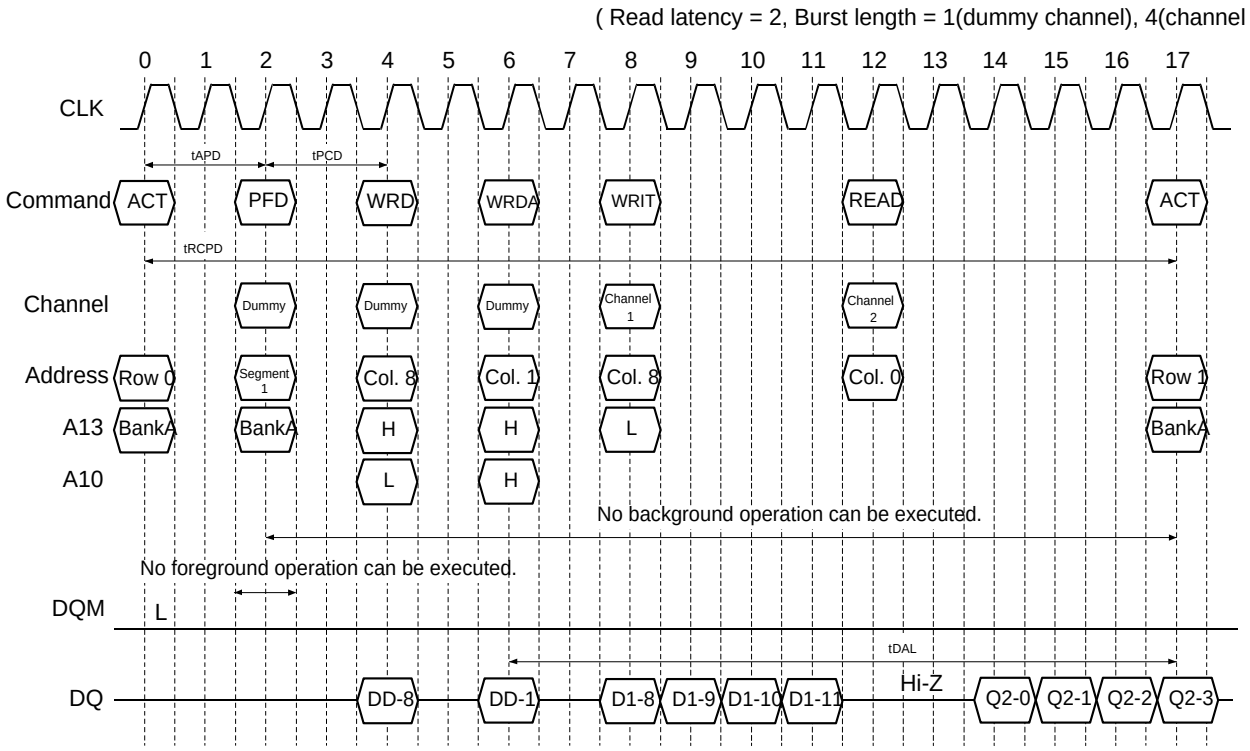


Figure 83
Pair Prefetch Operation

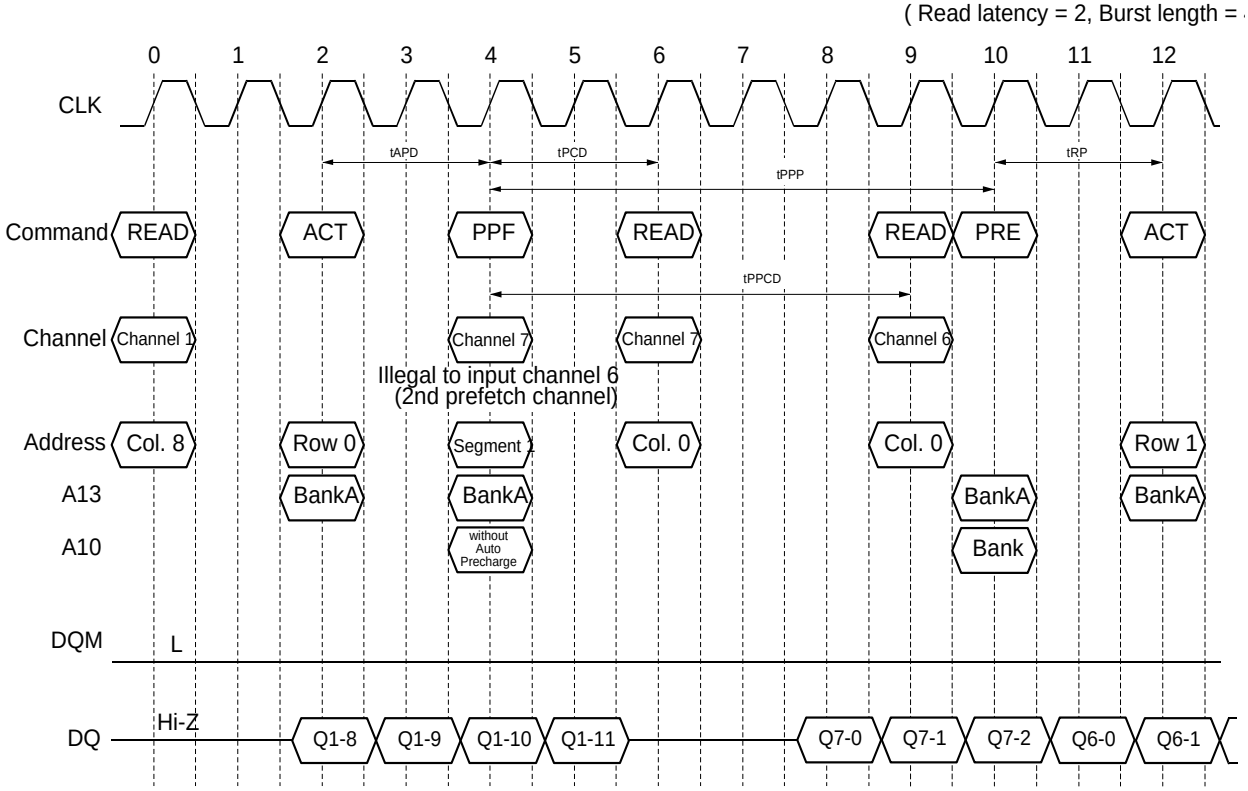


Figure 84
Pair Prefetch Operation with Auto Precharge

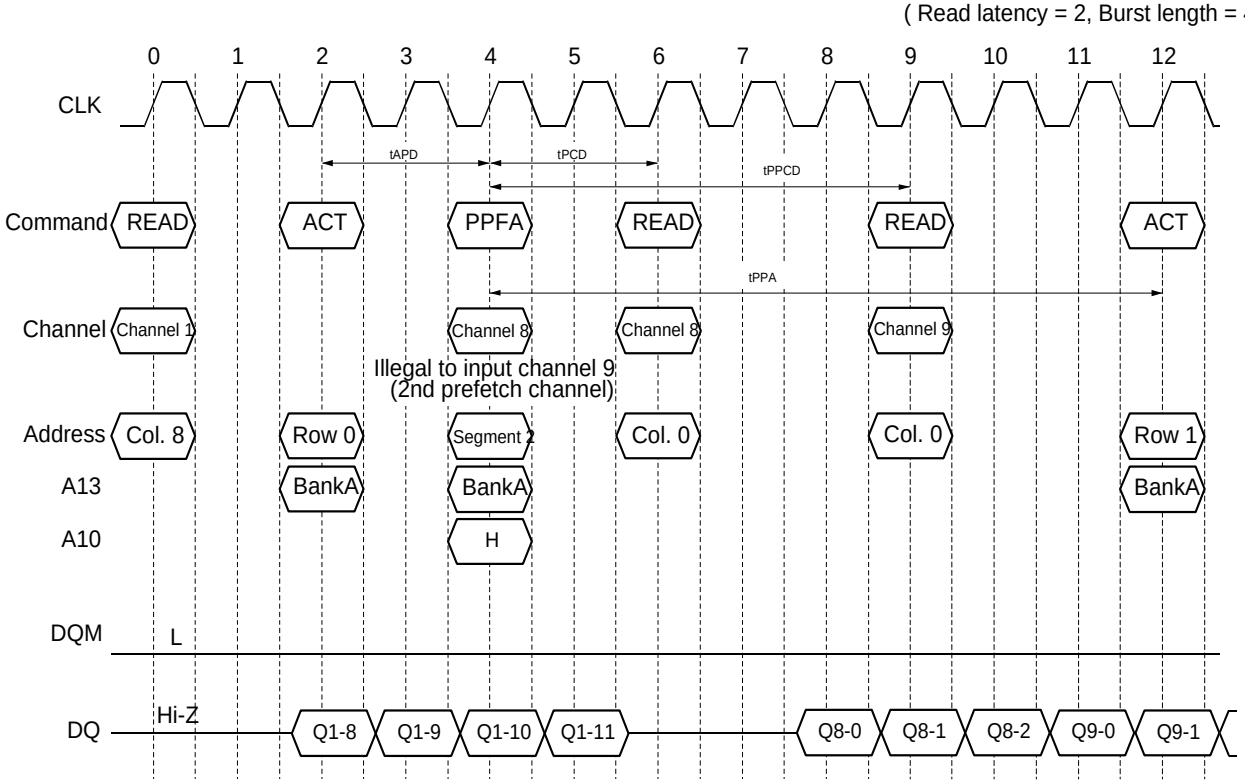


Figure 85
Pair Prefetch to Pair Prefetch Operation

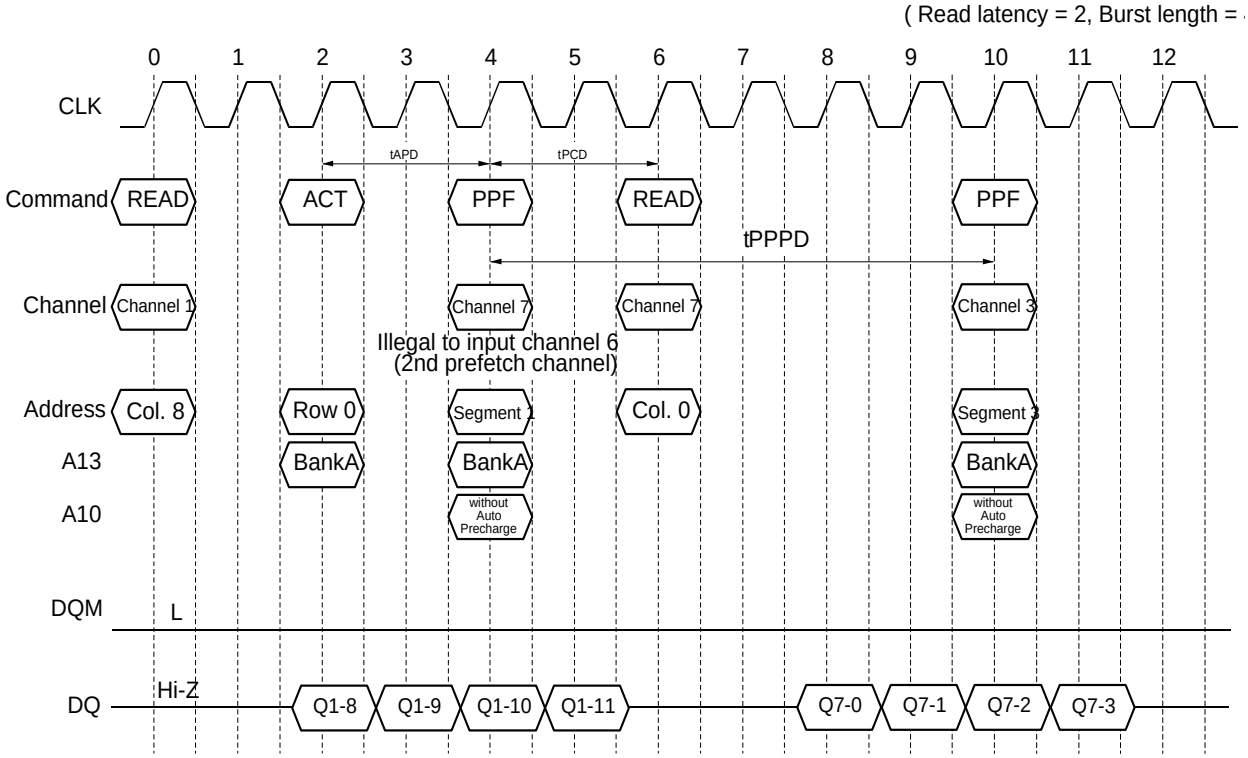


Figure 86
Read to Pair Prefetch to Write Operation (Same Channel Prefetch)

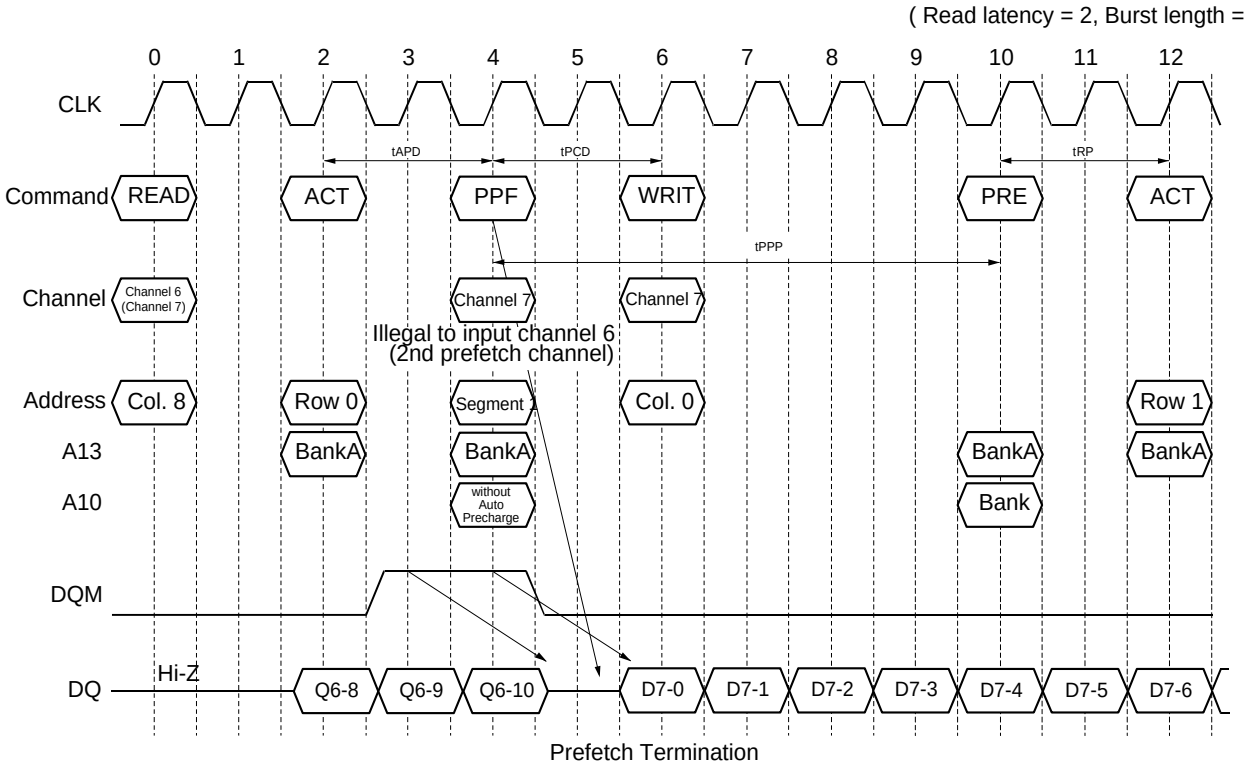


Figure 87
Auto Refresh Operation

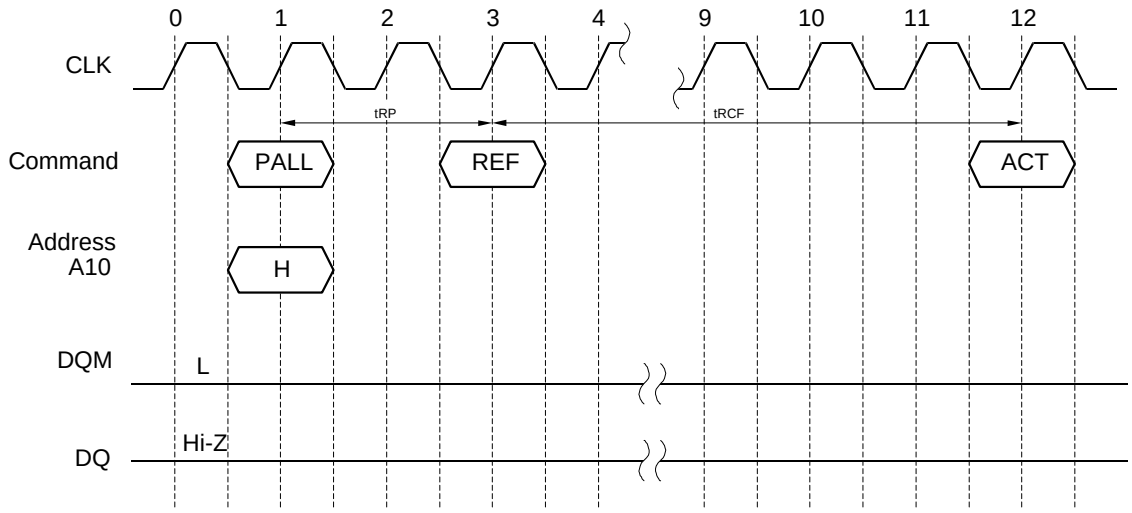
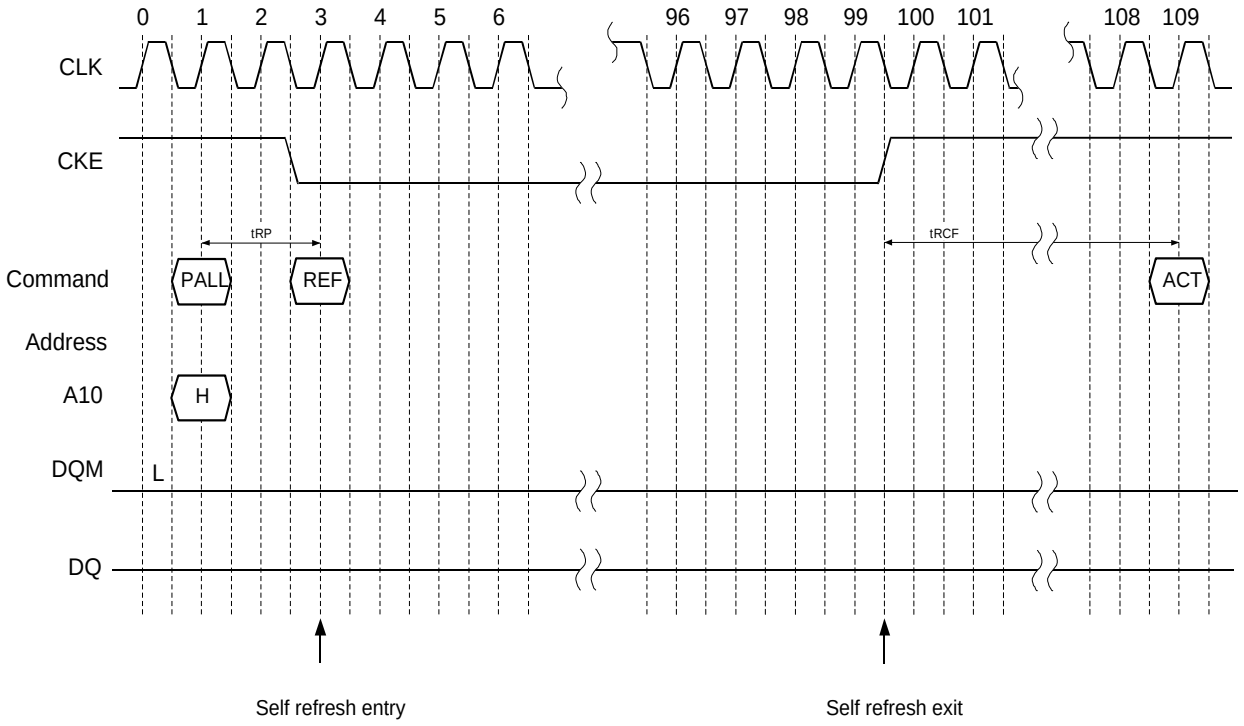


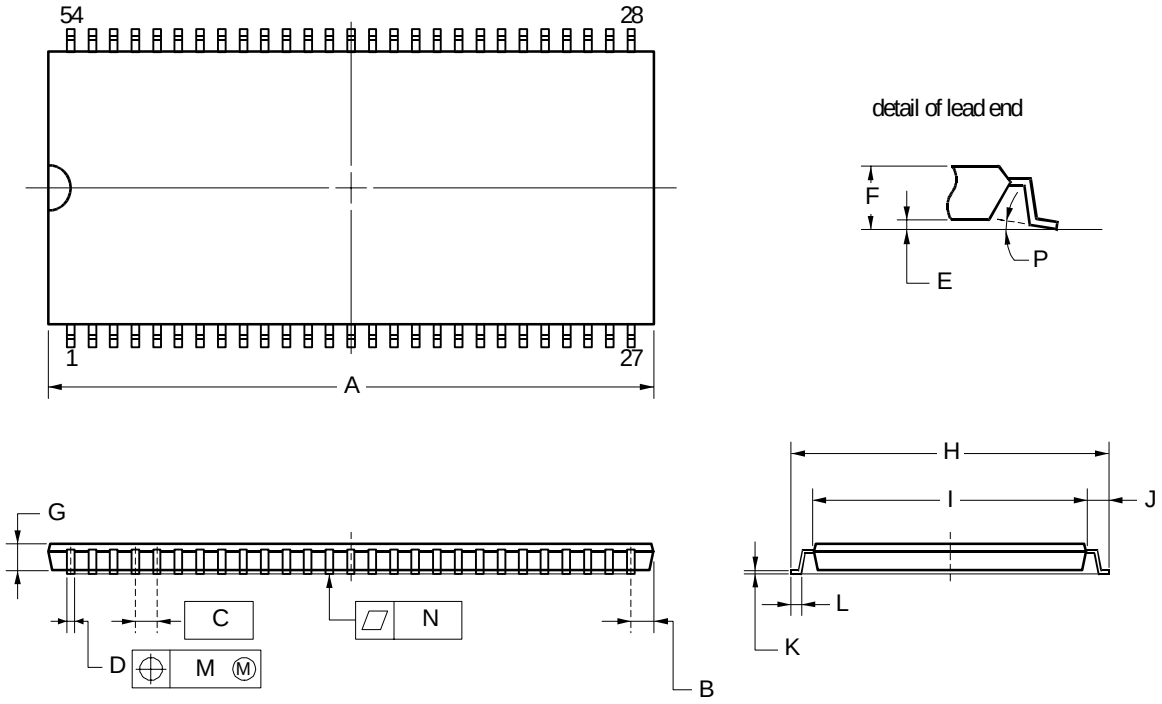
Figure 88
Self Refresh Operation (Entry and Exit)



5 Package

Figure 89
Package Drawing

54PIN PLASTIC TSOP (II) (400mil)



NOTE
Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	22.62 MAX.	0.891 MAX.
B	0.91 MAX.	0.036 MAX.
C	0.80 (T.P.)	0.031 (T.P.)
D	$0.32^{+0.08}_{-0.07}$	0.013±0.003
E	0.10±0.05	0.004±0.002
F	1.20 MAX.	0.048 MAX.
G	1.00	0.039
H	11.76±0.20	0.463±0.008
I	10.16±0.10	0.400±0.004
J	0.80±0.20	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.50±0.10	$0.020^{+0.004}_{-0.005}$
M	0.13	0.005
N	0.10	0.004
P	$3^{\circ}{}^{+7^{\circ}}_{3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{3^{\circ}}$